

1	2	3	4	5	6	7	8																																												
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HSF Property : Comply iSupplier SYSTEM HSF PROPERTY ATTRIBUTE UP-TO DATE VALUE PCB:6050A2498701		WWW.AliSaler.Com																																																	
RTL8165EH (10/100) LDO MODE R680:MOUNT R672:NA R14143:NA C741:NA C713:NA C12734:NA C12735:NA C12736:NA C12737:NA C12754:NA C12756:NA L332:NA U470:NA U9848:MOUNT 6016B0008001 U320:MOUNT 6019B0928301 R14131:NA		<h1>KF14BR</h1> <h2>AMD BRAZOS 2.0</h2> <h1>DB</h1>																																																	
RTL8161FH (GIGA-LAN) SWITCH MODE R680:NA R672:MOUNT 60130B0000ZT R14143:MOUNT 60130B00000Z C741:MOUNT C713:MOUNT C12734:MOUNT C12735:MOUNT C12736:MOUNT C12737:MOUNT C12754:MOUNT C12756:MOUNT L332:MOUNT U470:MOUNT 6016B0010601 U9848:NA U320:MOUNT 6019B0928101 R14131:MOUNT		<h1>2011/11/02</h1>																																																	
BOM CHANGE L332:6014B0200401		DB(MOUNT) X805:6018A0009301-004 C1329,C1303:6010A0036105 R1208,R1269:60130B10600Y R562:60130B10500Y X301:6018B0044501 C577,C578:6010071502AT C723,C724:6010B0010103 X304:6018B0044501		DB(OPEN) R16556 R16557 D321:6011A0026803 R14130		POWER BOARD :6050A2493201 USB BOARD :6050A2493701 PICK BUTTOM BOARD :6050A2493601																																													
<table border="1"> <tr><td>2011/06/20</td><td>2011-ECO-012815</td><td>B</td></tr> <tr><td>2011/03/21</td><td>2011-ECO-005030</td><td>A</td></tr> <tr><td>DATE</td><td>CHANGE NO.</td><td>REV</td></tr> </table>		2011/06/20	2011-ECO-012815	B	2011/03/21	2011-ECO-005030	A	DATE	CHANGE NO.	REV	<table border="1"> <tr> <td>EE</td><td>DATE</td><td>POWER</td><td>DATE</td><td rowspan="5"> INVENTEC TITLE SARAH BRAZOS </td> </tr> <tr> <td>DRAWER</td><td>ALAN WANG</td><td>2010-08-06</td><td>ALBERT</td> </tr> <tr> <td>DESIGN</td><td>ALAN WANG</td><td>2010-08-06</td><td>ALBERT</td> </tr> <tr> <td>CHECK</td><td></td><td></td><td></td> </tr> <tr> <td>RESPONSIBLE</td><td></td><td></td><td></td> </tr> <tr> <td colspan="4"> SIZE = 3 VER : A02 </td> <td> SIZE CODE A3 CS </td> <td> DOC. NUMBER 1310A24127-0-MTR </td> <td> REV B </td> </tr> <tr> <td colspan="4"> FILE NAME : BRAZOS-6050A2412701 P/N 6050A2412701 </td> <td> SHEET 1 </td> <td> OF 54 </td> <td></td> </tr> </table>						EE	DATE	POWER	DATE	INVENTEC TITLE SARAH BRAZOS	DRAWER	ALAN WANG	2010-08-06	ALBERT	DESIGN	ALAN WANG	2010-08-06	ALBERT	CHECK				RESPONSIBLE				SIZE = 3 VER : A02				SIZE CODE A3 CS	DOC. NUMBER 1310A24127-0-MTR	REV B	FILE NAME : BRAZOS-6050A2412701 P/N 6050A2412701				SHEET 1	OF 54	
2011/06/20	2011-ECO-012815	B																																																	
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FILE NAME : BRAZOS-6050A2412701 P/N 6050A2412701				SHEET 1	OF 54																																														
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 40- HP and MIC CONN
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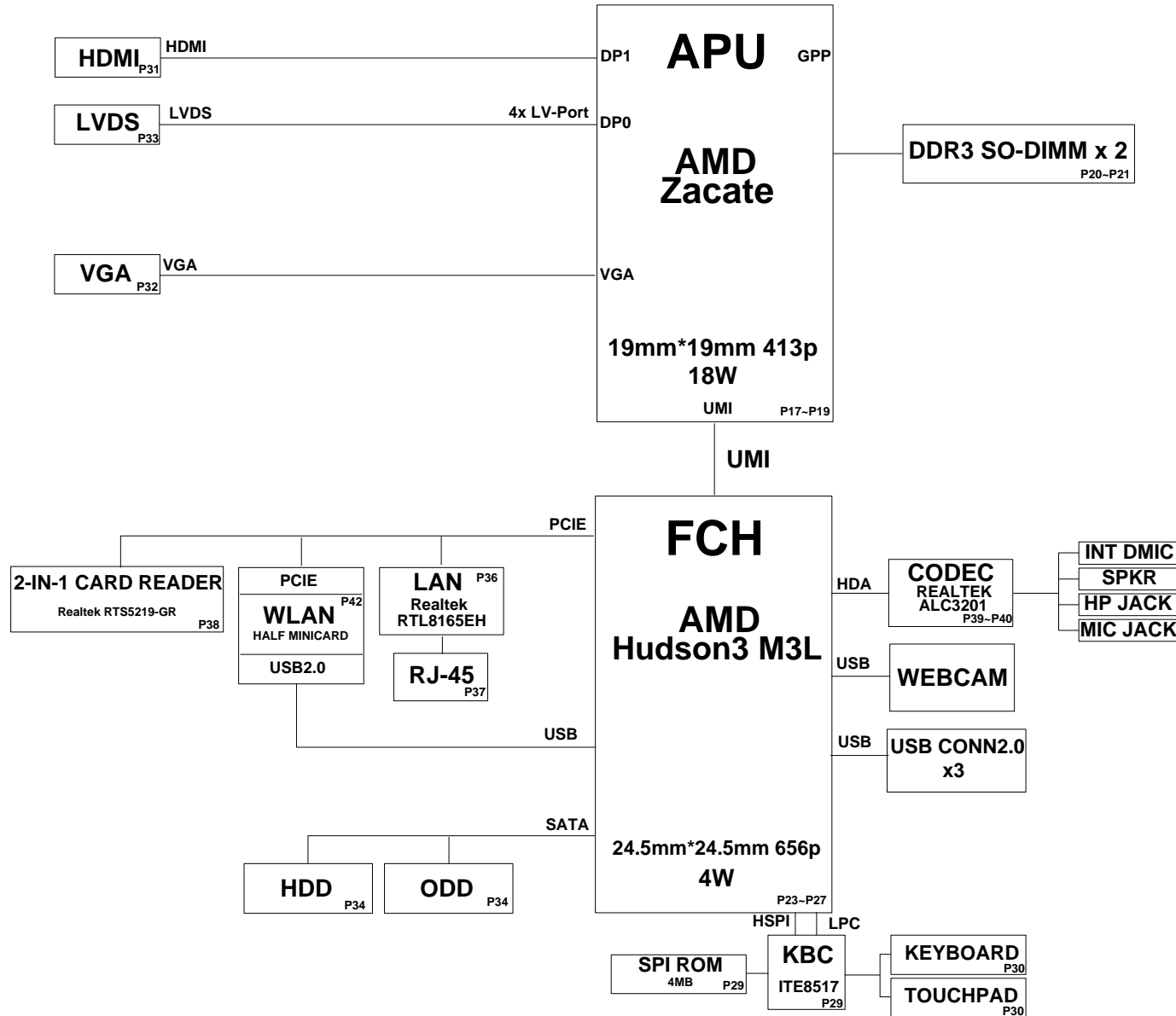
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Sarah 15.6 Brazos Index			
SIZE	CODE	DOC. NUMBER	REV
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CHANGE by	Chang, Irene	4-Oct-2011	SHEET	2	OF	45
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Brazos

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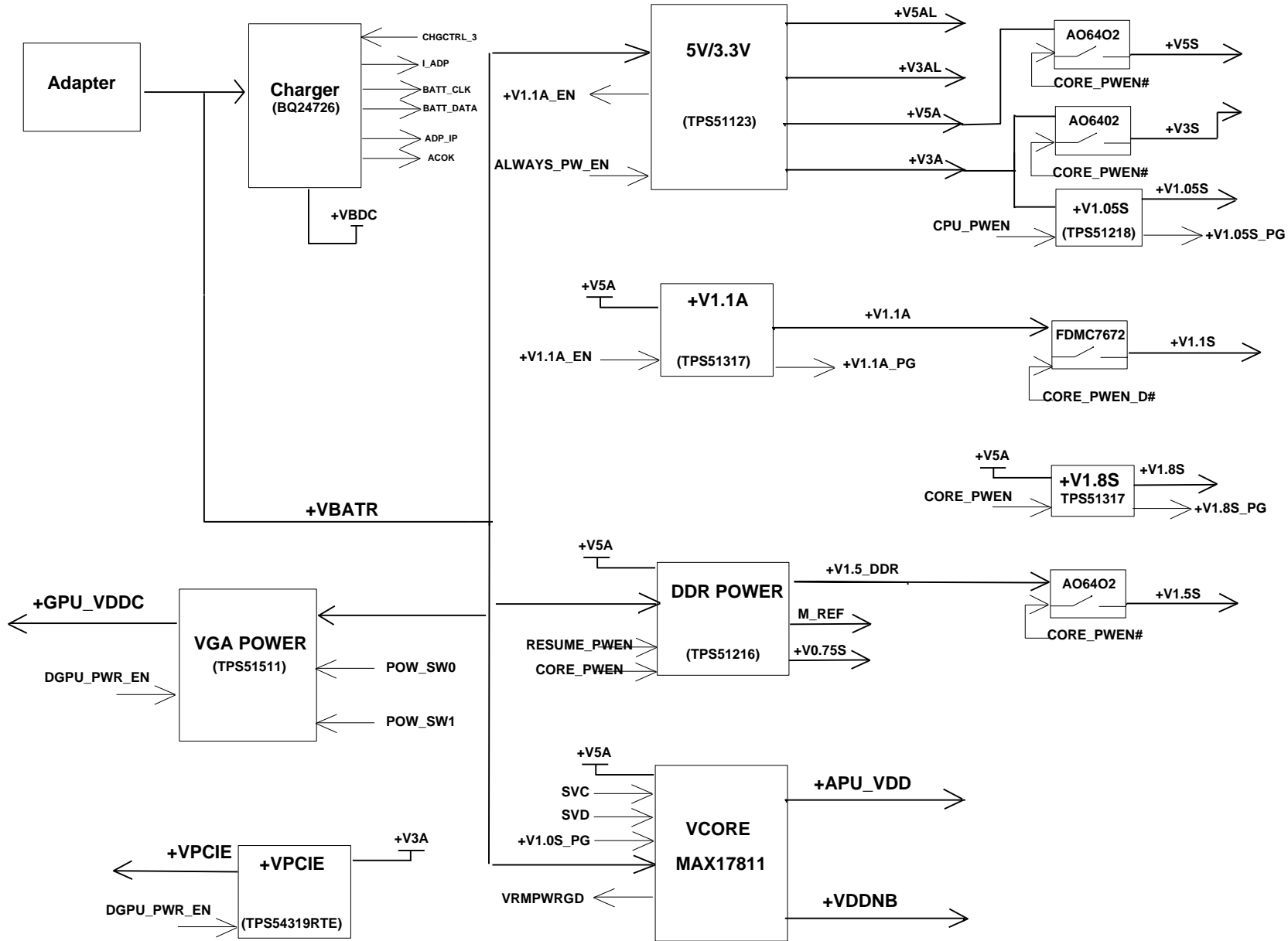
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Block Diagram

SIZE	CODE	DOC. NUMBER	REV
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CHANGE by: Chang, Irene 4-Oct-2011

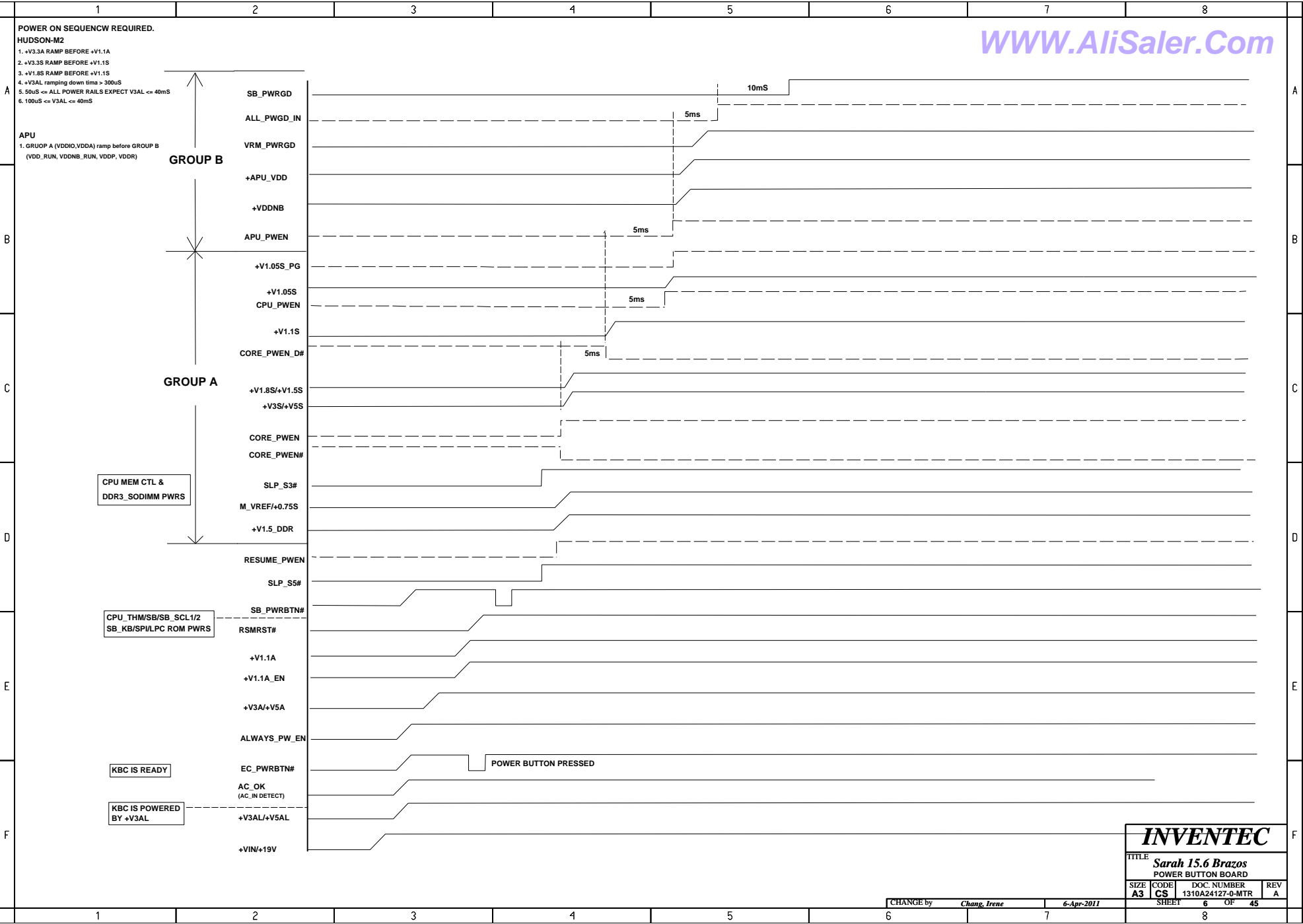
SHEET 3 OF 45

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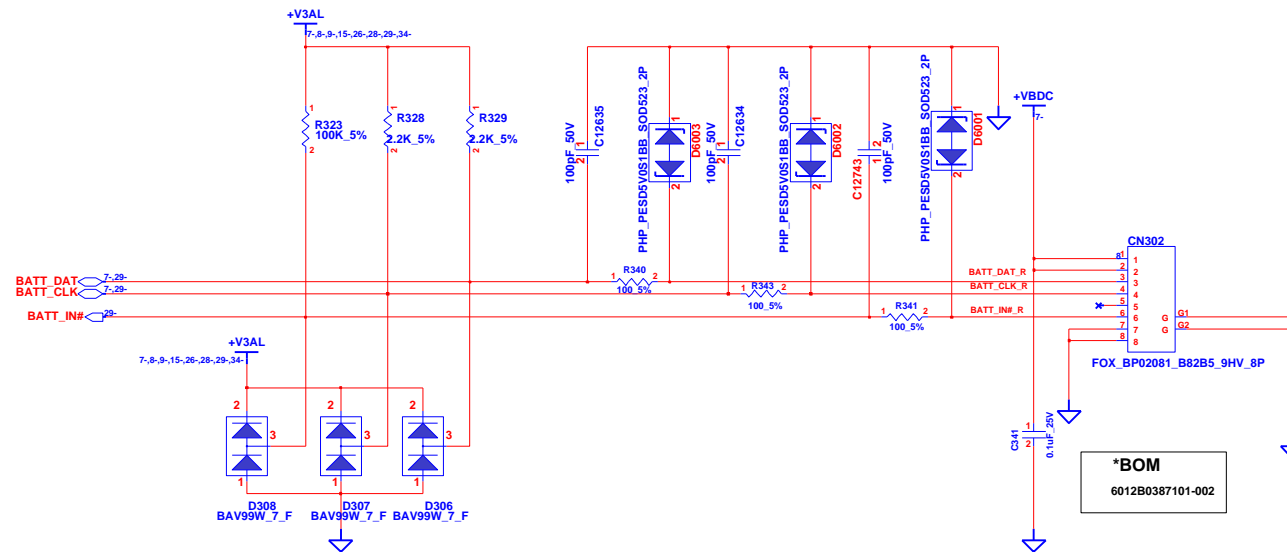
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TITLE Sarah 15.6 Brazos			
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SHEET 4		OF 45	

CHANGE by Chang, Irene 6-Apr-2011

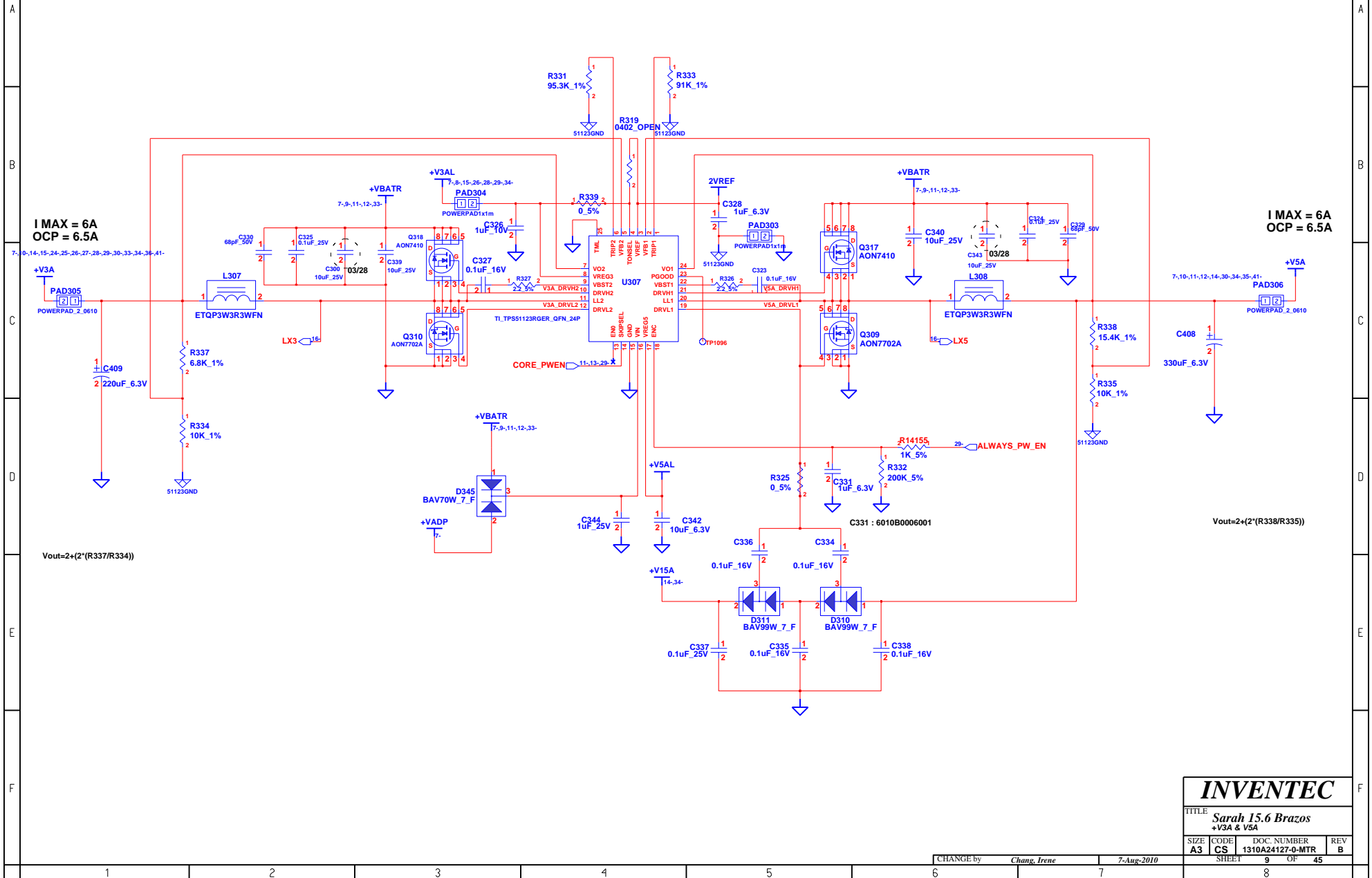




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SHEET 3 OF 15			



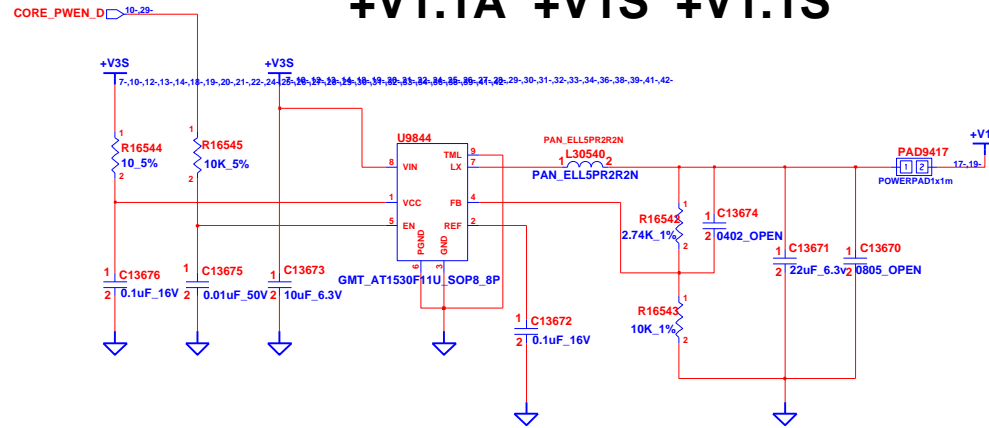
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TITLE Sarah 15.6 Brazos BATTERY CONN			
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CHANGE by Chang, Irene		24-Dec-2010	
SHEET 8		OF 45	



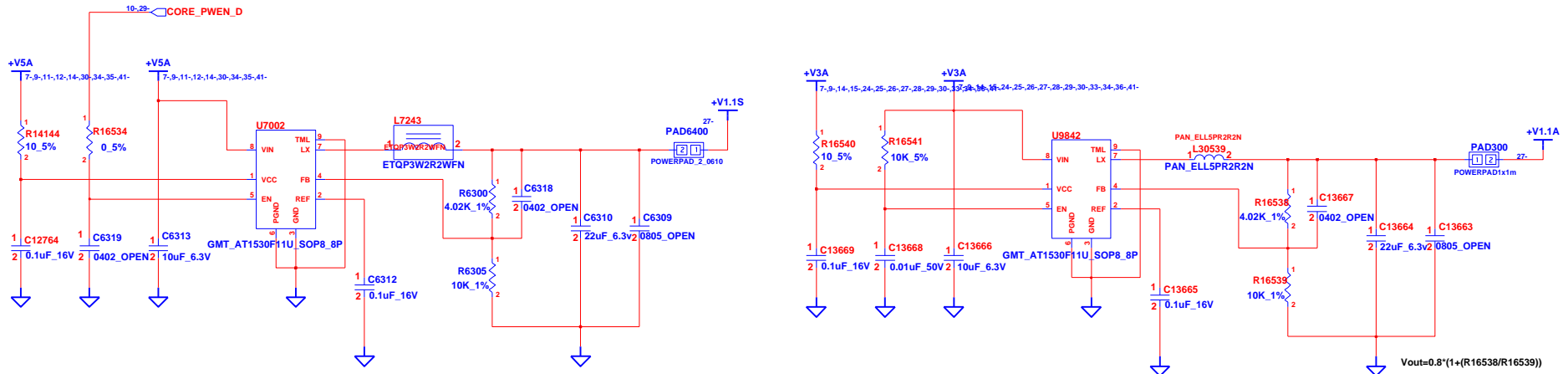
INVENTEC

TITLE			
Sarah 15.6 Brazos			
+V3A & V5A			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B
CHANGE by		Chang, Irene	7-Aug-2010
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+V1.1A +V1S +V1.1S



$$V_{out}=0.8*(1+(R16542/R16543))$$



$$V_{out}=0.8*(1+(R6300/R6305))$$

INVENTEC			
TITLE: KF14BR-SCHE-DB-20110928-M3L			
SIZE: A3	CODE: CS	DOC. NUMBER:	REV:
SHEET: 10		OF: 45	

CHANGE by: KF14BR 29-Sep-2011

[illegible][illegible][illegible][illegible][illegible]

$$V_{out}=0.8*(1+(R_{14145}/R_{14146}))$$

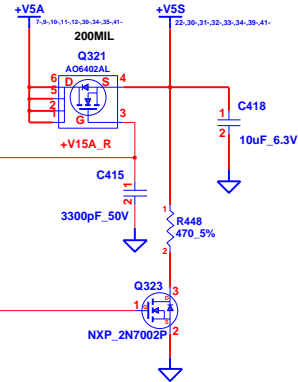
INVENTEC

TITLE	<i>Sarah 15.6 Brazos</i> +V1.0S &+V1.8S
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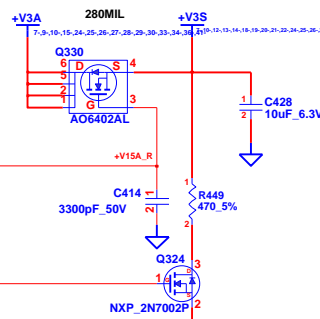
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SHEET 13 OF 45			

CHANGE by	<i>Chang, Irene</i>	<i>10-Aug-2011</i>
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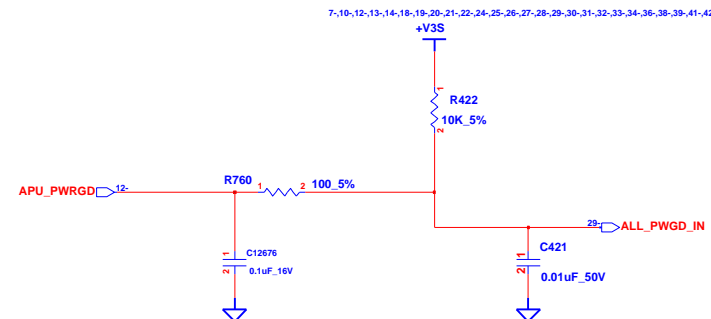
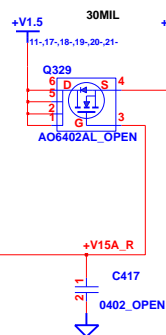
I MAX = 2.7A



I MAX = 3.3A



I MAX = 0.8A



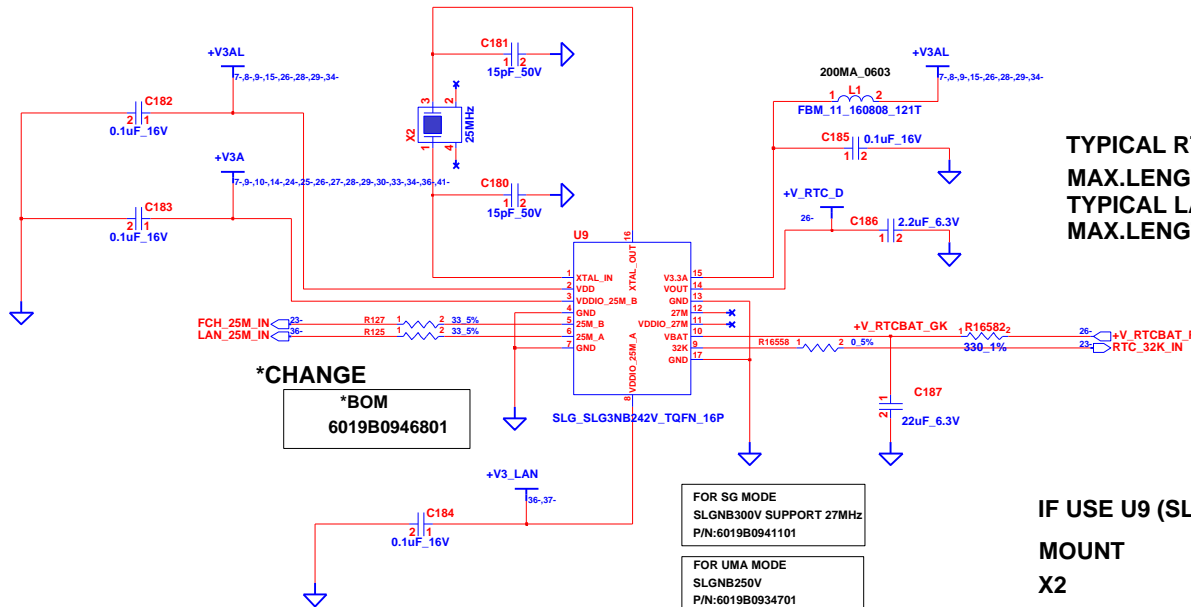
CORE_PWEN#	+V15A_R	+V3S / +V5S
LOW	HIGH	V3S & V5S
HIGH	LOW	0V

CORE_PWEN#	+V15A_R	+V1.5S
LOW	HIGH	+V1.5S
HIGH	LOW	0V

INVENTEC

TITLE			
Sarah 15.6 Brazos			
+V3S & +V5S & +V1.5S & +V1.1S			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B
SHEET		14	OF 45

CHANGE by Chang, Irene 28-Mar-2011



TYPICAL RTC_32K IN TRACE <=6
MAX.LENGTH<=24
TYPICAL LAN_25M IN TRACE <=8
MAX.LENGTH<=12

***CHANGE**
***BOM**
6019B0946801

FOR SG MODE
SLGNB300V SUPPORT 27MHz
P/N:6019B0941101

FOR UMA MODE
SLGNB250V
P/N:6019B0934701

IF USE U9 (SLG3NB250V)

MOUNT

X2

R1

C180

C181

C182

C183

C184

C185

C186

C187

R16557(PAGE23)

R16556(PAGE23)

R14130(PAGE36)

OPEN(PAGE26)

D321

OPEN(PAGE23)

R1208

R1269

X805

C1303

C1329

OPEN(PAGE36)

C723

C724

X304

R14130

OPEN(PAGE23)

X304

C724

C723

OPEN(PAGE23)

R562

X301

C577

C578

INVENTEC

TITLE
Sarah 15.6 Brazos
+VDDC_GPU & +V1.0_DGPU

SIZE CODE DOC NUMBER REV
A3 CS 1310A24127-0-MTR B

CHANGE by Chang, Irene 23-Sep-2011

SHEET 15 OF 45

	1	2	3	4	5	6	7	8	
A	<div><div>RF</div><div><div><div><div>LX3</div><div><div><div>1</div><div>2</div></div><div><div>R439</div><div>0402_OPEN</div></div><div><div>C435</div><div>0402_OPEN</div></div></div></div><div><div>LX5</div><div><div><div>1</div><div>2</div></div><div><div>R438</div><div>0402_OPEN</div></div><div><div>C434</div><div>0402_OPEN</div></div></div></div><div><div>LXMEM</div><div><div><div>1</div><div>2</div></div><div><div>R452</div><div>4.7_5%</div></div><div><div>C454</div><div>2200pF_50V</div></div></div></div><div><div>LXCHG</div><div><div><div>1</div><div>2</div></div><div><div>R14164</div><div>4.7_5%</div></div><div><div>C12656</div><div>2200pF_50V</div></div></div></div></div></div></div>								
B									
C									
D									
E									
F									
	1	2	3	4	5	6	7	8	

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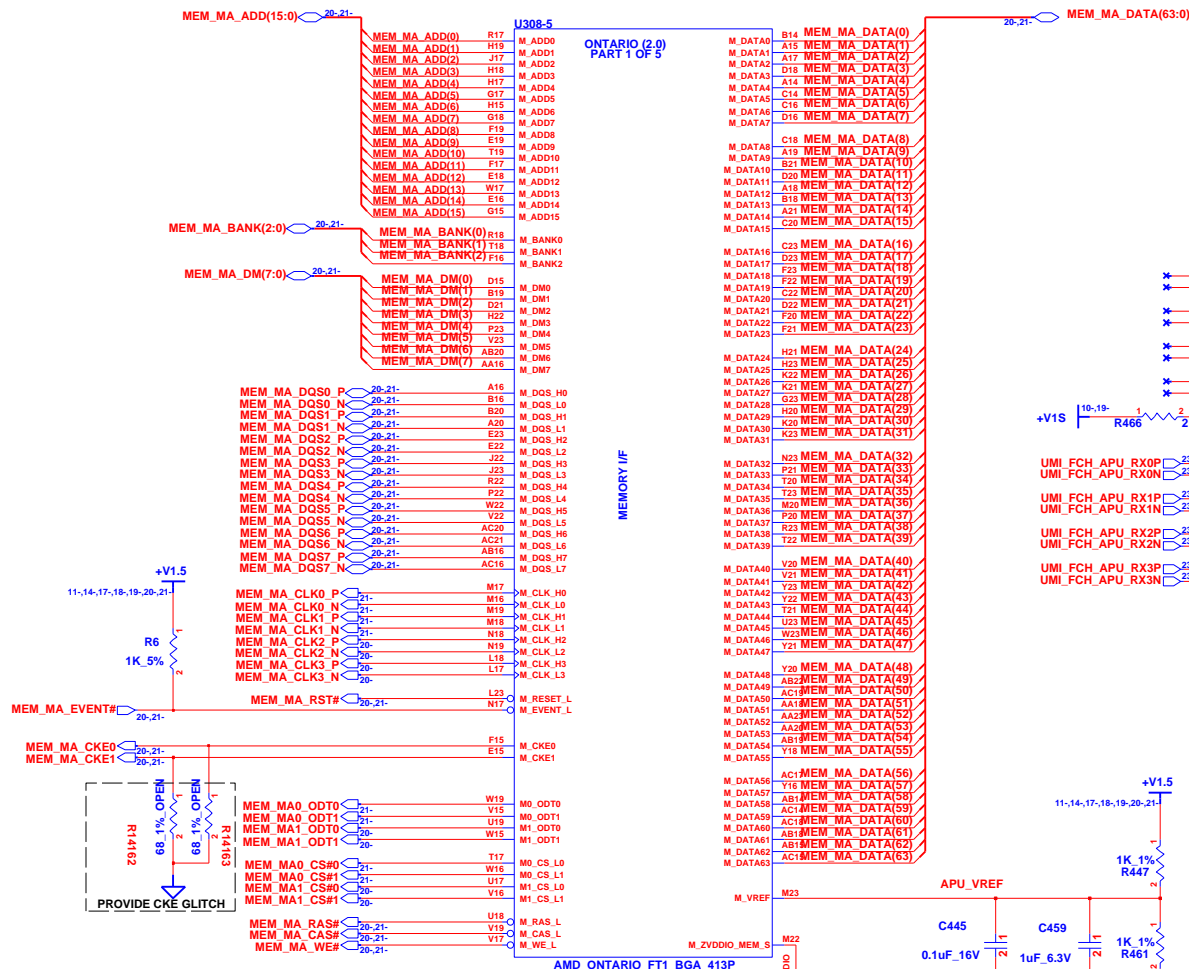
INVENTEC

TITLE Sarah 15.6 Brazos
CHECK

SIZE A3	CODE CS	DOC. NUMBER 1310A24127-0-MTR	REV B
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CHANGE by	Chang, Irene	31-Aug-2010	SHEET 16 OF 45
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The diagram illustrates the U308-1 chip, labeled "ONTARIO (2.0) PART 2 OF 5", which is a PCIe IF and UMI IF controller. It is connected to various components as follows:

- Power and Ground:**
 - V1S:** Connected to the 10-19 pin header via R466 (2K, 1%) and ON_ZVDD.
 - P_ZVDD_10:** Connected to the 10-19 pin header via R466 (2K, 1%) and ON_ZVDD.
 - P_ZVSS:** Connected to the 10-19 pin header via R465 (27K, 1%) and ON_ZVSS.
- PCIe IF:**
 - P_GPP_RXP0, P_GPP_RXN0:** Connected to AB6 and AC6.
 - P_GPP_RXP1, P_GPP_RXN1:** Connected to AB4 and AC4.
 - P_GPP_RXP2, P_GPP_RXN2:** Connected to AA1 and AA2.
 - P_GPP_RXP3, P_GPP_RXN3:** Connected to YA and Y3.
 - P_GPP_TXP0, P_GPP_TXN0:** Connected to AB6 and AC6.
 - P_GPP_TXP1, P_GPP_TXN1:** Connected to AB3 and AC3.
 - P_GPP_TXP2, P_GPP_TXN2:** Connected to Y1 and Y2.
 - P_GPP_TXP3, P_GPP_TXN3:** Connected to V3 and V4.
- UMI IF:**
 - U_MLI_RXP0, U_MLI_RXN0:** Connected to AA2 and Y12.
 - U_MLI_RXP1, U_MLI_RXN1:** Connected to AA10 and Y10.
 - U_MLI_RXP2, U_MLI_RXN2:** Connected to AB10 and AC10.
 - U_MLI_RXP3, U_MLI_RXN3:** Connected to AC7 and AB7.
 - U_MLI_TXP0, U_MLI_TXN0:** Connected to AB12 and AC12.
 - U_MLI_TXP1, U_MLI_TXN1:** Connected to AC11 and AB11.
 - U_MLI_TXP2, U_MLI_TXN2:** Connected to AA8 and Y8.
 - U_MLI_TXP3, U_MLI_TXN3:** Connected to AB8 and AC8.
- Other Connections:**
 - UMI_APU_FCH_TX0P, UMI_APU_FCH_TX0N:** Connected to C432 and C430.
 - UMI_APU_FCH_TX1P, UMI_APU_FCH_TX1N:** Connected to C432 and C429.
 - UMI_APU_FCH_TX2P, UMI_APU_FCH_TX2N:** Connected to C439 and C437.
 - UMI_APU_FCH_TX3P, UMI_APU_FCH_TX3N:** Connected to C438 and C436.

Route A-LINK DIFF PAIR @85 OHM+/- 10%

Net Name	Target Impedance	Routing Dimensions	Spacing to Other	Self Spacing
CLK	72 ohm	0.2 / 0.1 / 0.2	0.5	0.5
ADD	40 ohm	0.2	0.2	0.3
DQS	90 ohm	0.1 / 0.1 / 0.1	0.4	0.4
Data/DM	40 ohm	0.2	0.3	0.3

R460 connection to +V1.5 should be directly to the plane without a long trace.

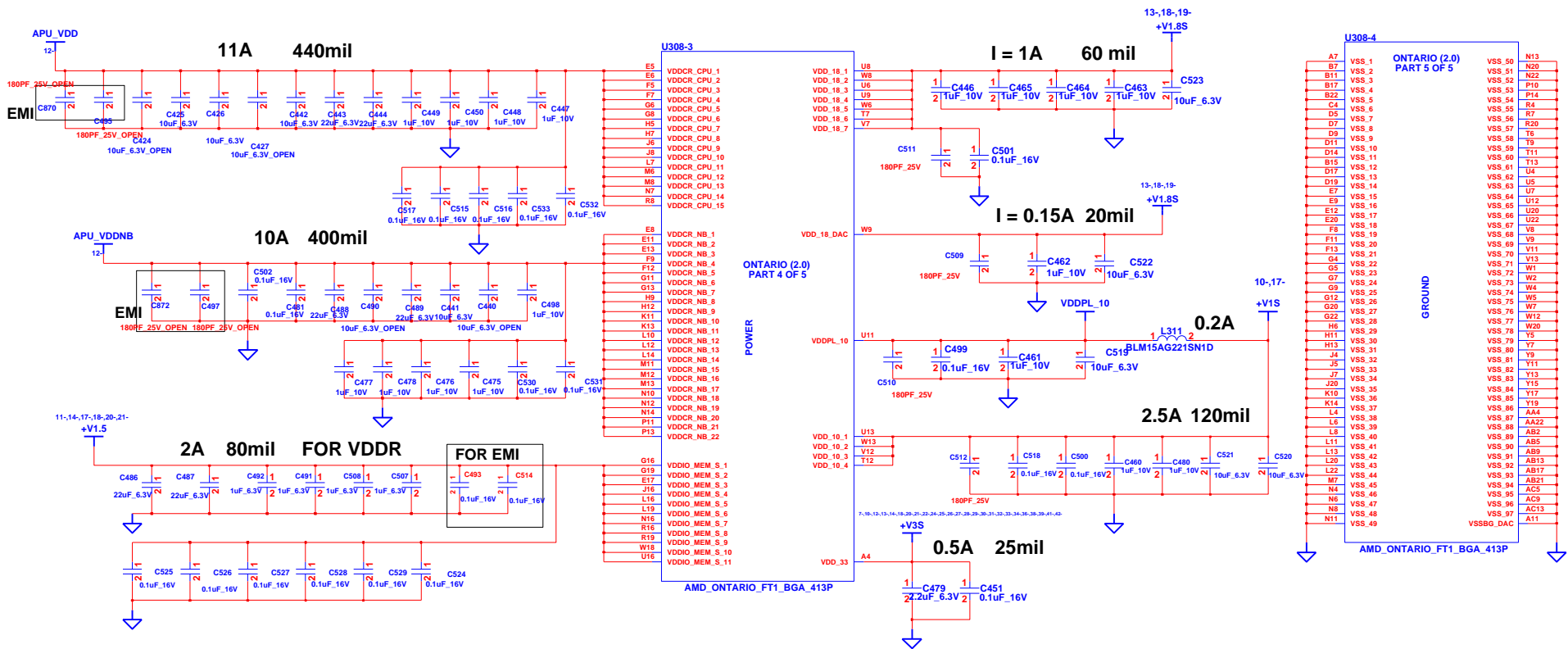
TITLE			
<i>Sarah 15.6 Brazos</i>			
CPU-1			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B

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APU

POWER / GND



INVENTEC

TITLE: Sarah 15.6 Brazos CPU-4			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A24127-0-MTR	REV: B
SHEET: 19		OF: 45	

CHANGE by: Chang, Irene 7-Aug-2010

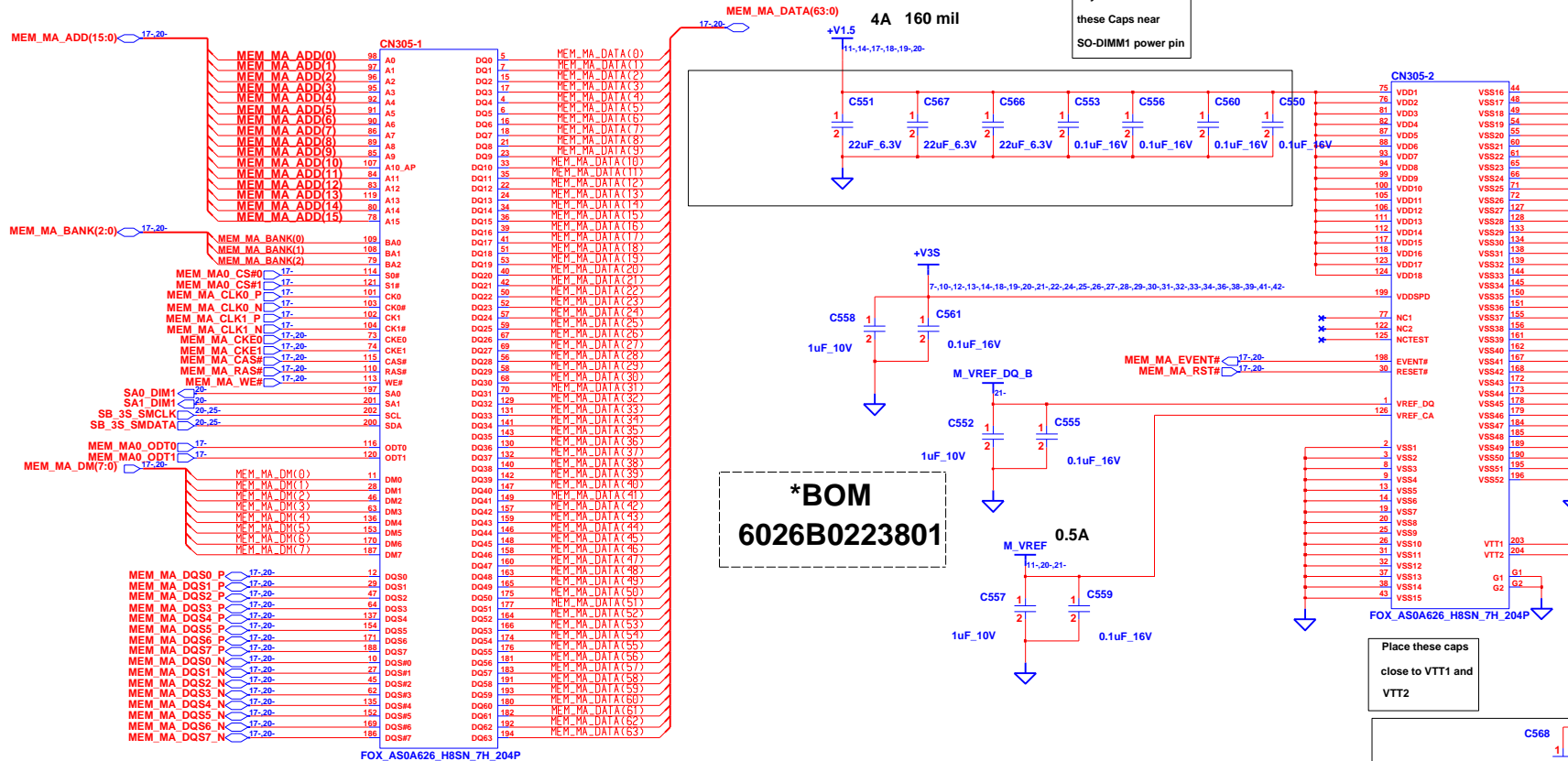
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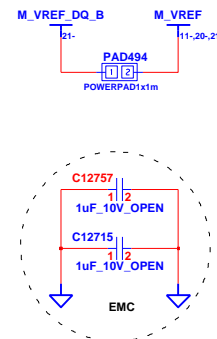
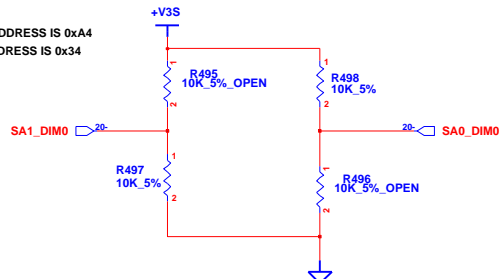
SO-DIMM1

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Layout Note: Place these Caps near SO-DIMM1 power pin



NOTE:
SO-DIMM SPD ADDRESS IS 0xA4
SO-DIMM TS ADDRESS IS 0x34



INVENTEC

TITLE: Sarah 15.6 Brazos
DDR3 DIMM1

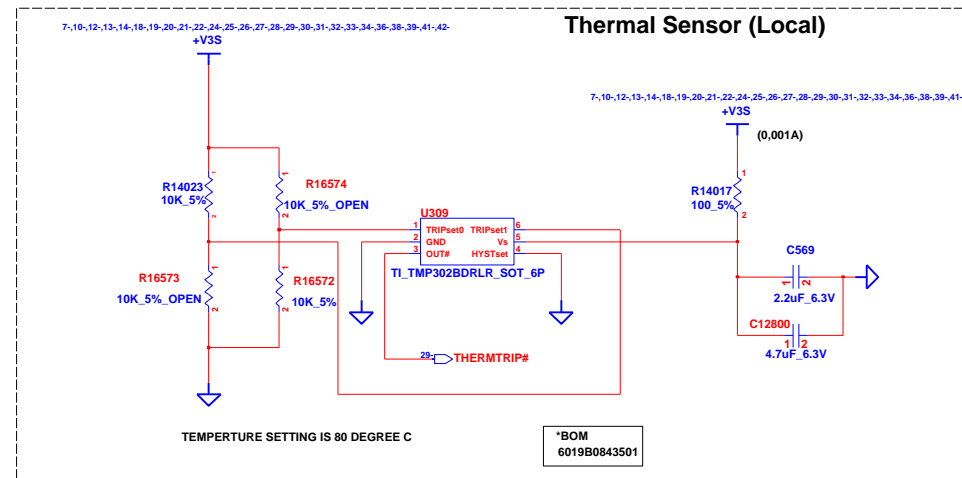
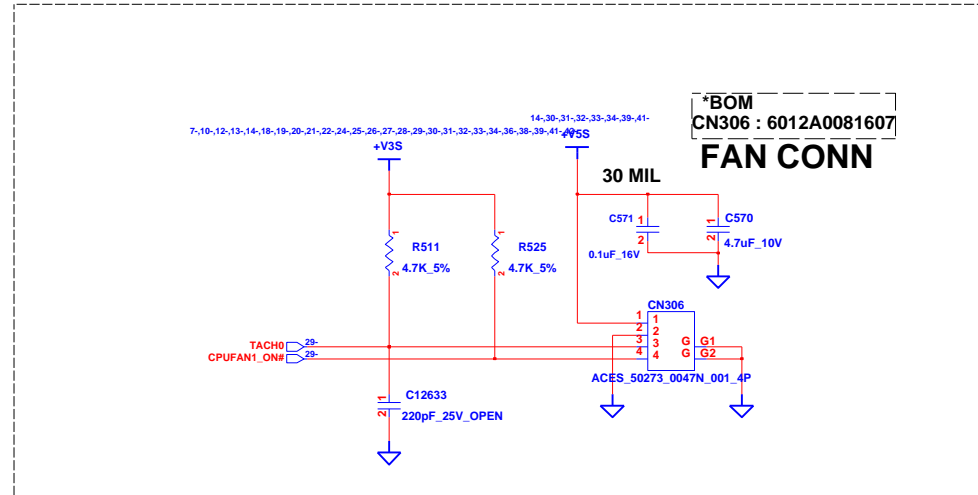
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A3	CS	1310A24127-0-MTR	B

CHANGE by: Chang, Irene 23-Feb-2011

SHEET 21 OF 45

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OK



INVENTEC

TITLE
Sarah 15.6 Brazos
FAN & THERMAL

SIZE CODE DOC NUMBER REV
A3 CS 1310A24127-0-MTR B

CHANGE by *Chang, Irene* 13-Oct-2010

SHEET 22 OF 45

FCH

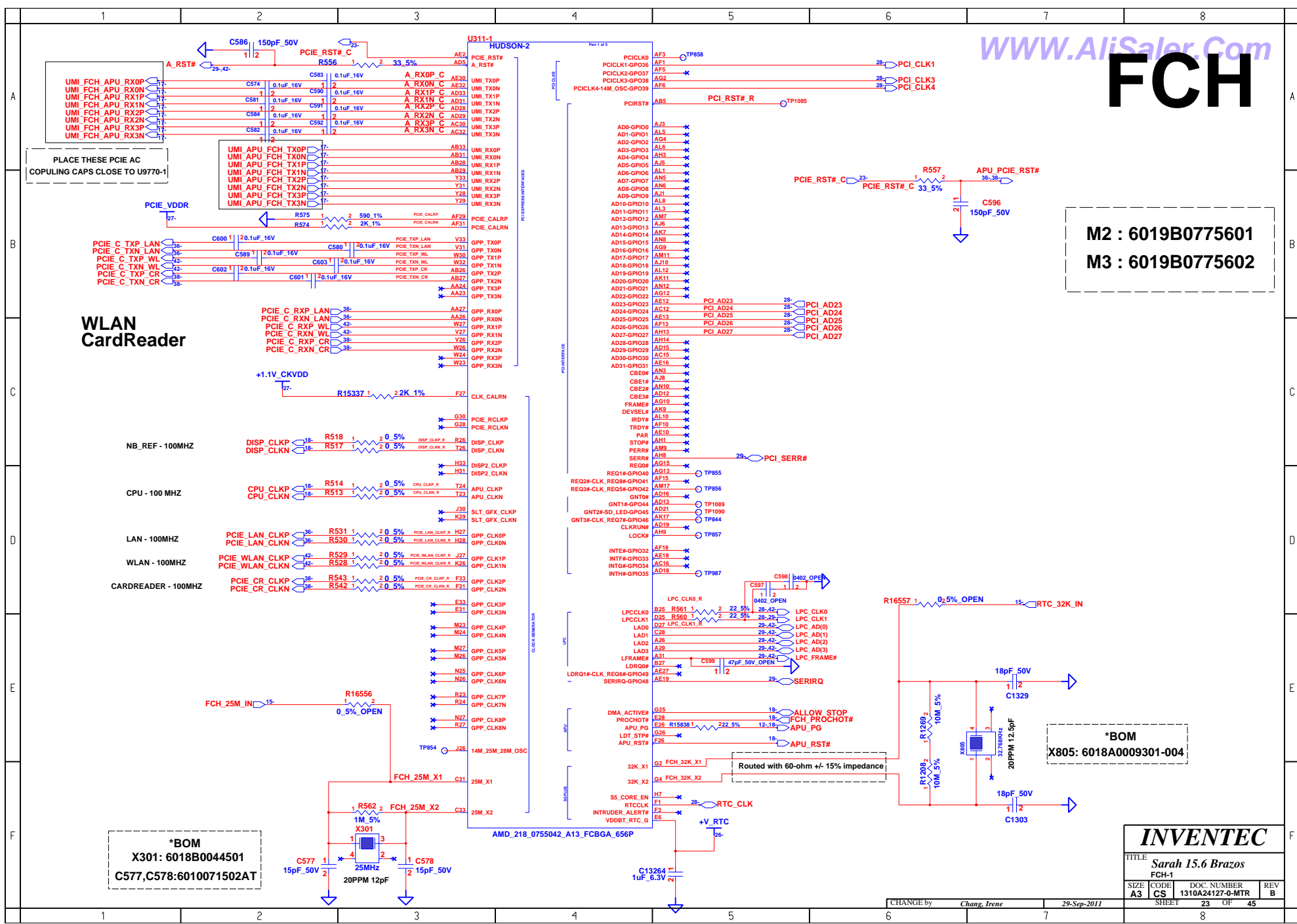
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M3 : 6019B0775602

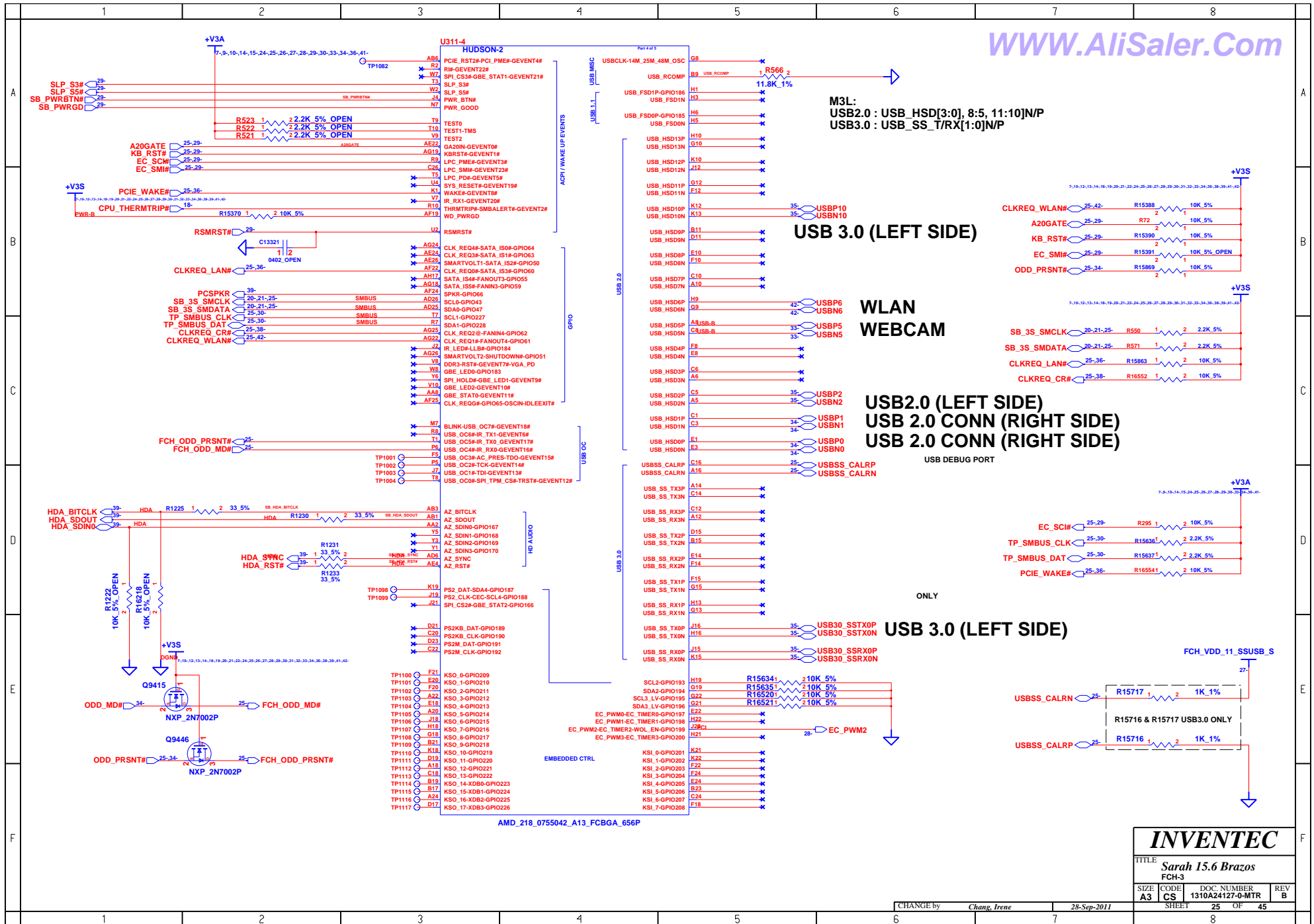
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X805: 6018A0009301-004

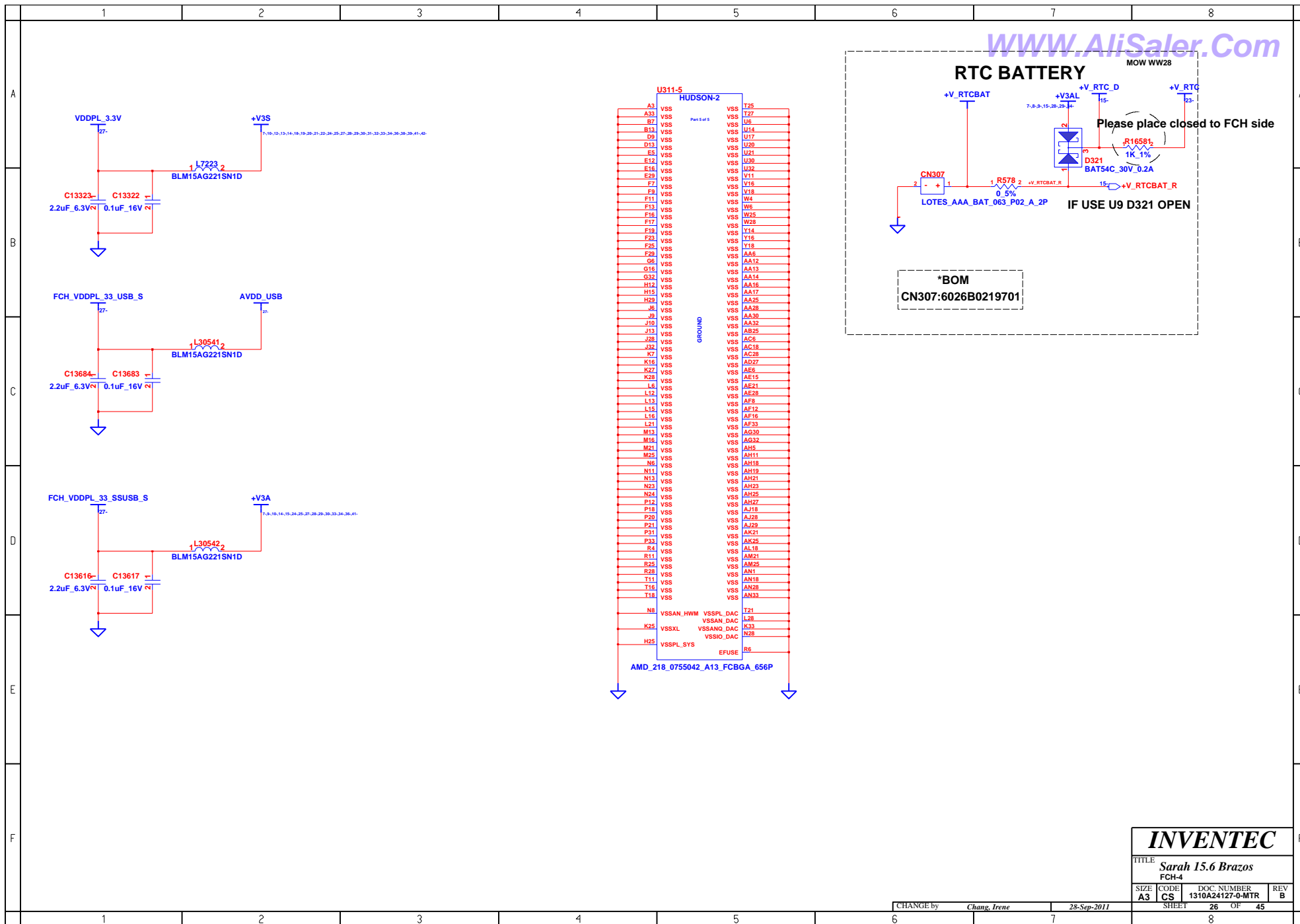
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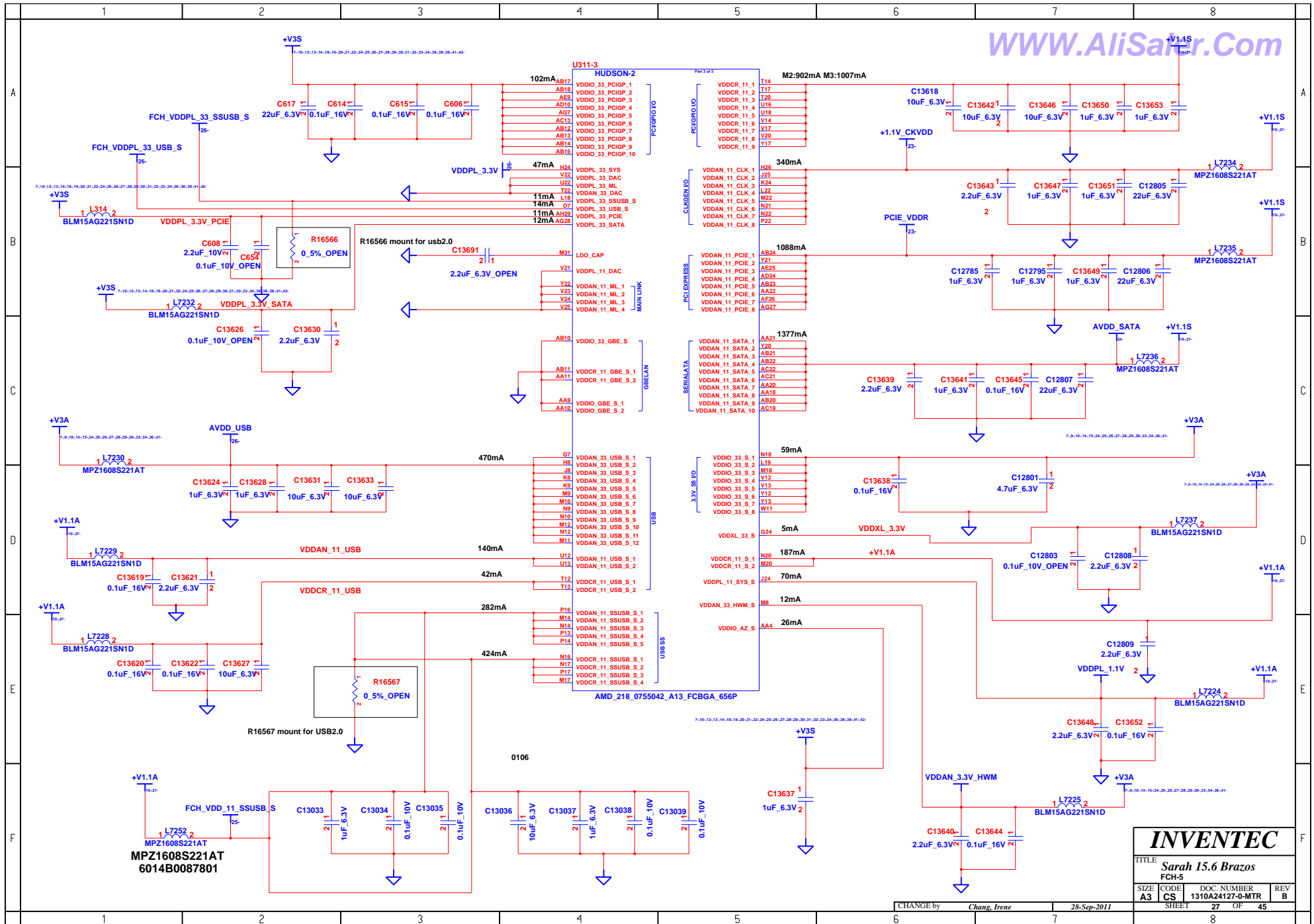
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FCH-1			
SIZE A3	CODE CS	DOC NUMBER 1310A24127-0-MTR	REV B
SHEET 23		OF 45	

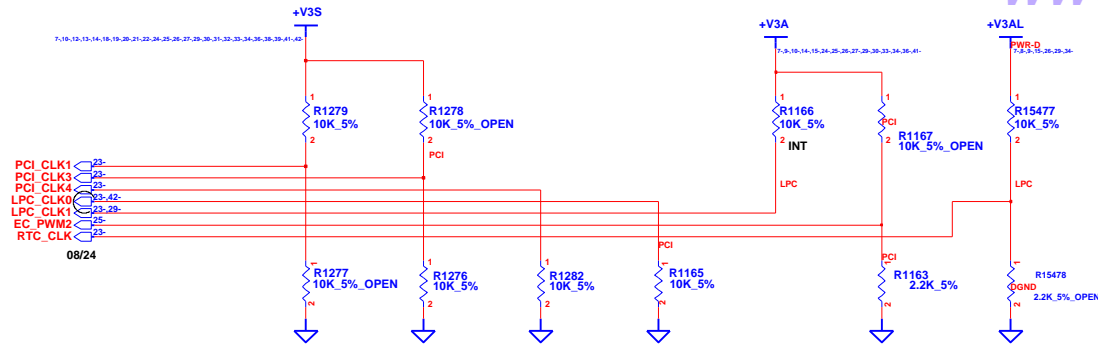
CHANGE by Chang, Irene 29-Sep-2011





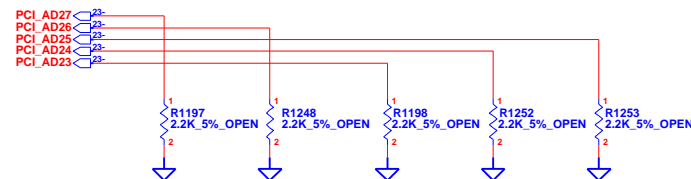






Required Straps:

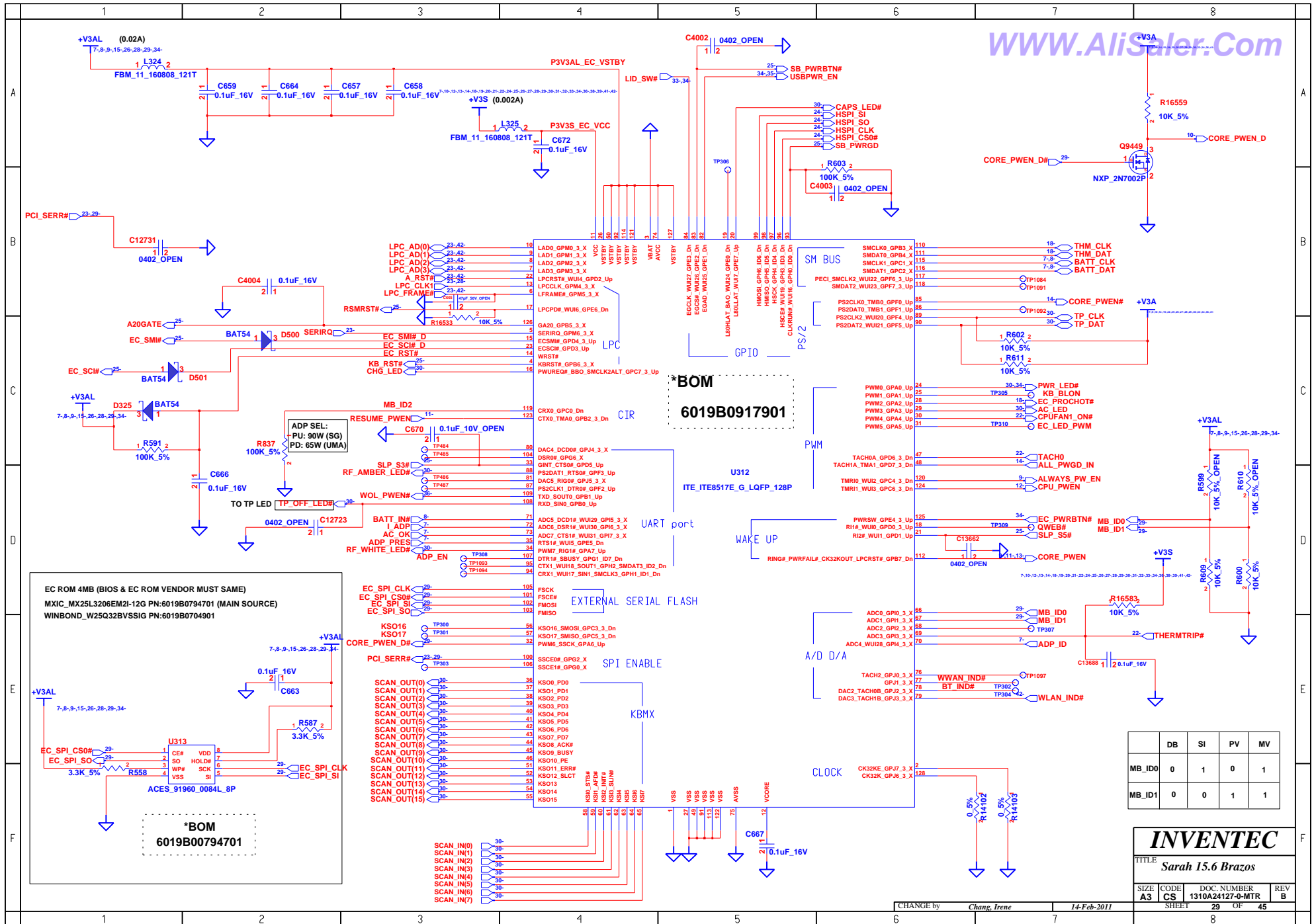
RTCCCLK		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2
S5 PLUS MODE DISABLE (DEFAULT)	PULL HIGH	ALLOW PCIE Gen2 DEFAULT	USE DEBUG STRAP	non Fusion CLOCK MODE APU_CLK AND DISP_CLK NO CLOCK OUTPUT	EC ENABLED	INTEGRATED CLKGEN ENABLED DEFAULT	LPC ROM
S5 PLUS MODE ENABLE	PULL LOW	FORCE PCIE Gen1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK MODE DEFAULT APU_CLK AND DISP_CLK CLOCK OUTPUT FROM INT CLOCK GEN	EC DISABLED DEFAULT	INTEGRATED CLKGEN DISABLED	SPI ROM DEFAULT



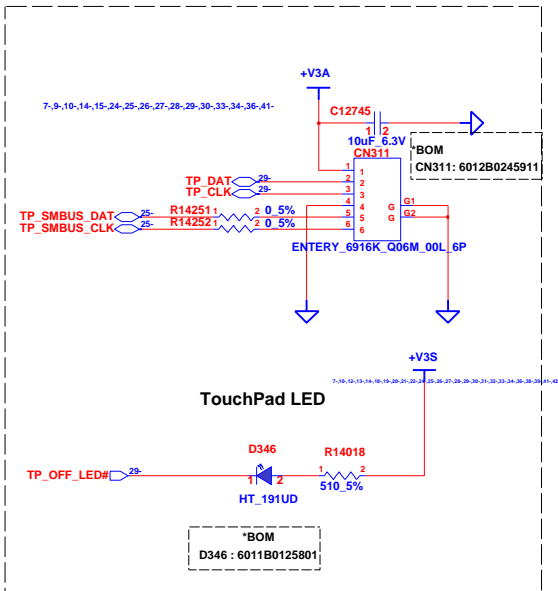
Debug Straps

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (default)	DISABLE ILA AUTORUN (default)	USE FC PLL (default)	USE DEFAULT PCIE STRAPS (default)	DISABLE PCI MEM BOOT (default)
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PCI PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

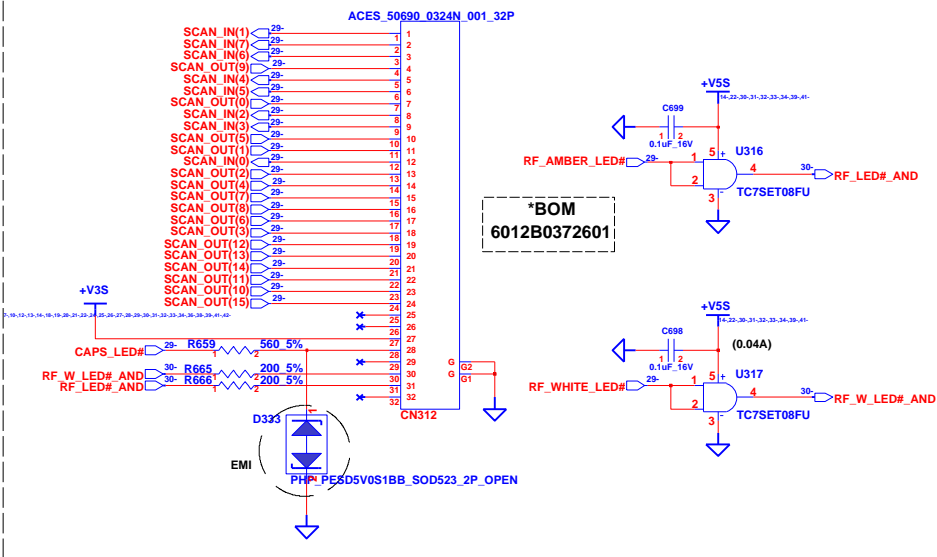


TouchPad Module CONN

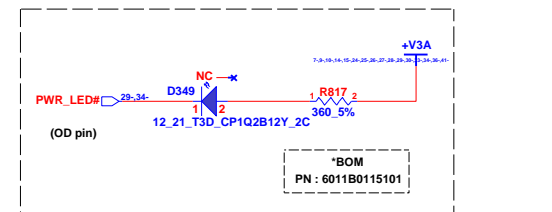
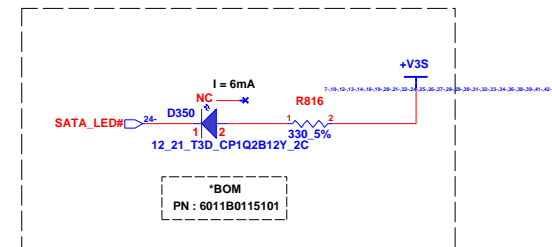
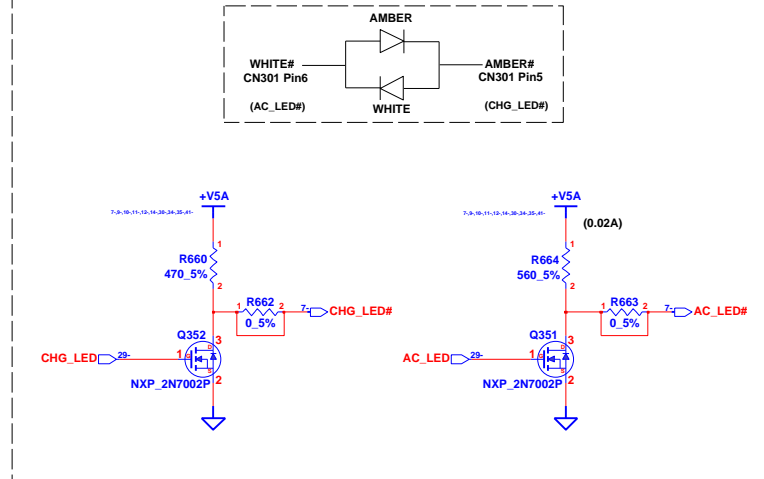


TouchPad LED

KeyBoard CONN (30 pin)



DC-JACK LED



INVENTEC

TITLE
Sarah 15.6 Brazos
KBC

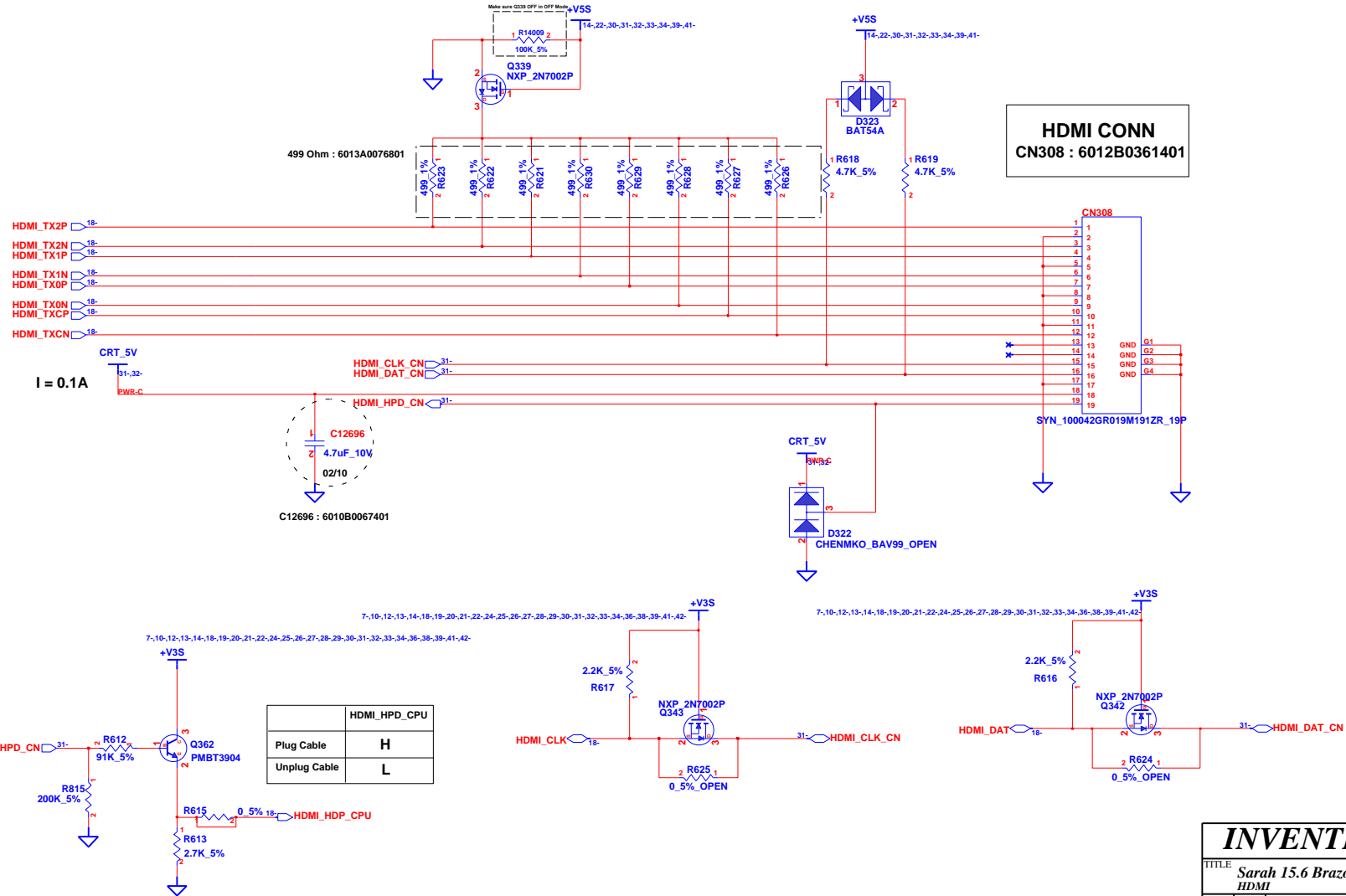
SIZE CODE DOC. NUMBER REV
A3 CS 1310A24127-0-MTR B

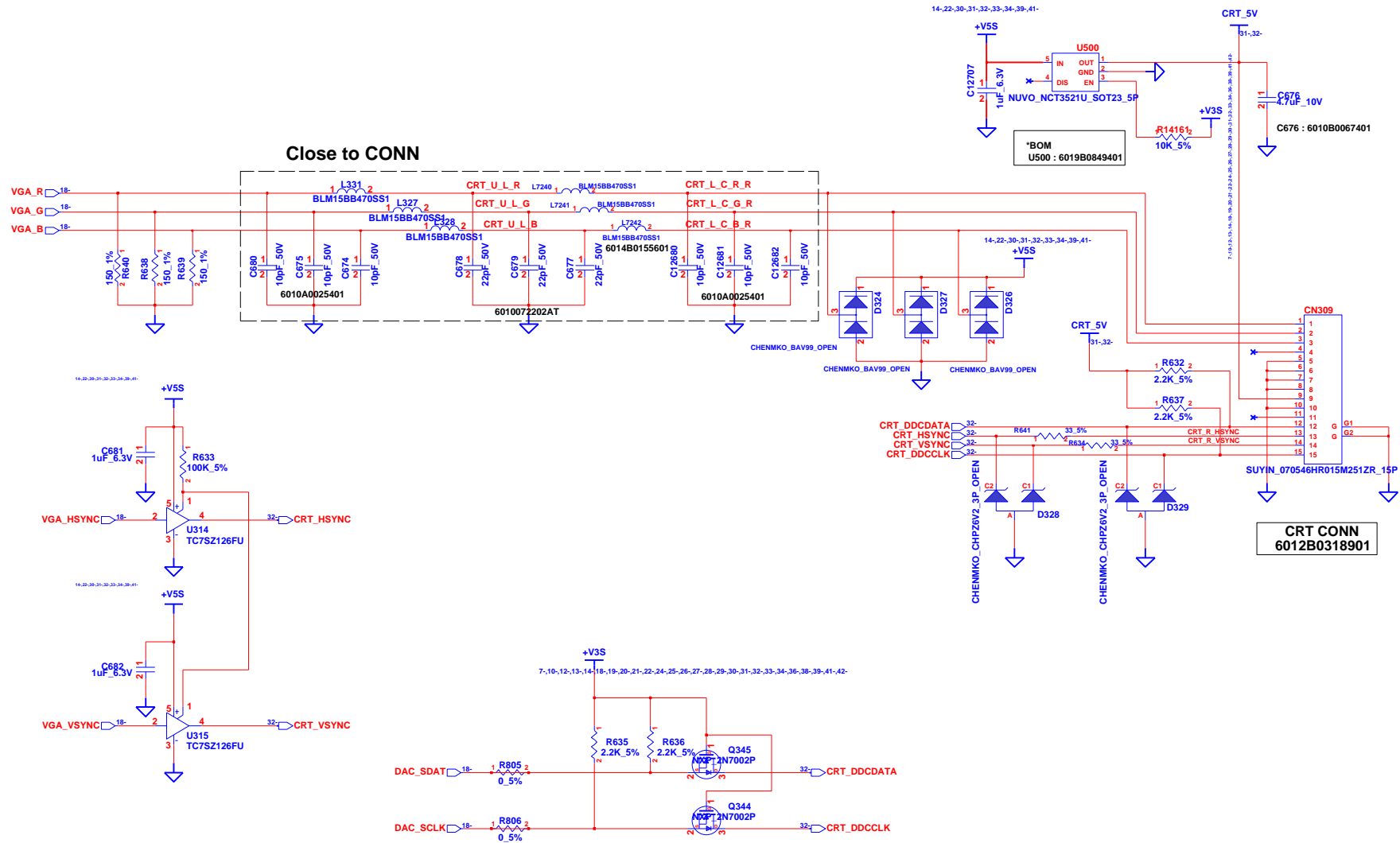
CHANGE by Chang, Irene 7-Aug-2010

SHEET 30 OF 45

HDMI

OK





INVENTEC

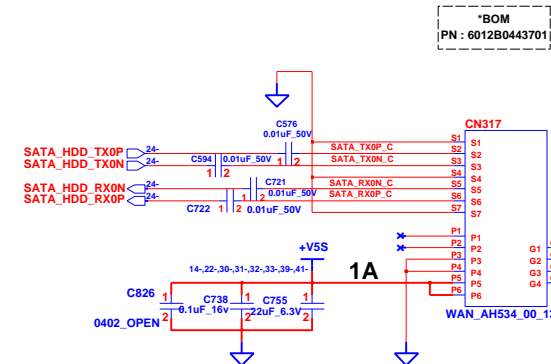
TITLE: Sarah 15.6 Brazos CRT

SIZE A3	CODE CS	DOC. NUMBER 1310A24127-0-MTR	REV B
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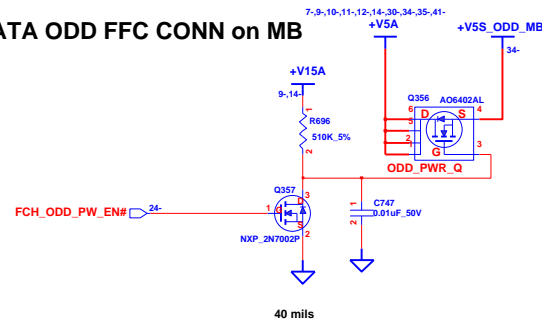
CHANGE by Chang, Irene 12-Mar-2011

SHEET 32 OF 45

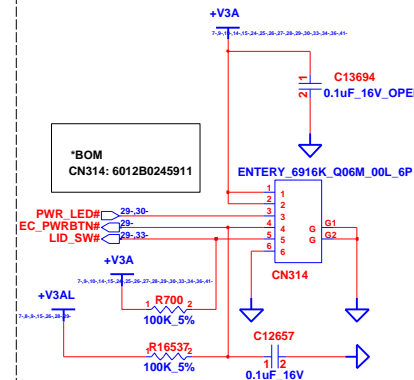
SATA HDD FFC CONN on MB



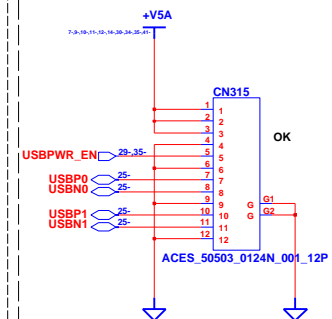
SATA ODD FFC CONN on MB



PBN Cable CN on MB



USB BOARD Cable on MB

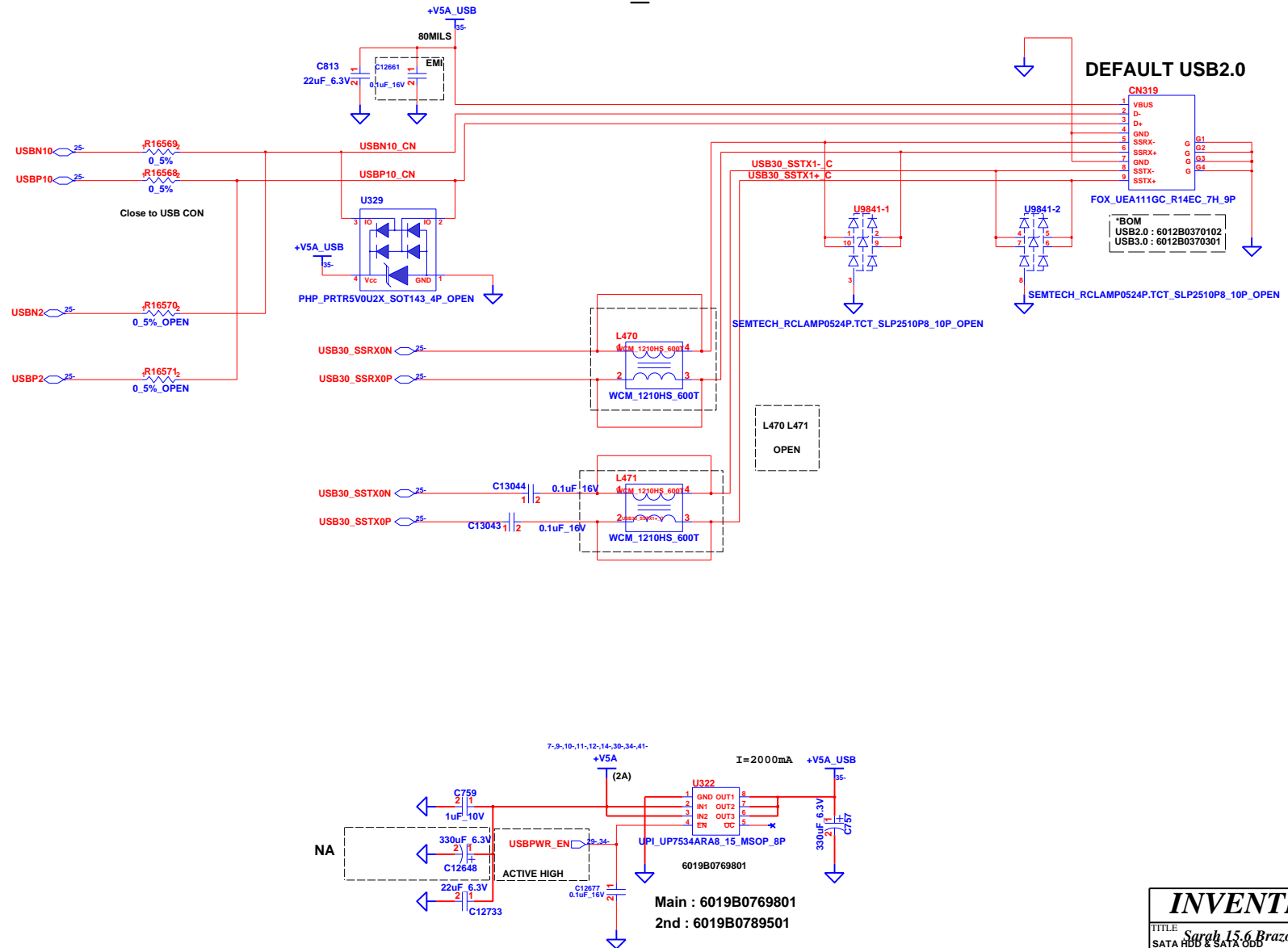


INVENTEC

TITLE: Sarah 15.6 Brazos			
KB CONN & TP CONN & Indicate LED			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A24127-0-MTR	REV: B
SHEET: 34		OF: 45	

CHANGE by: Chang, Irene 24-Dec-2010

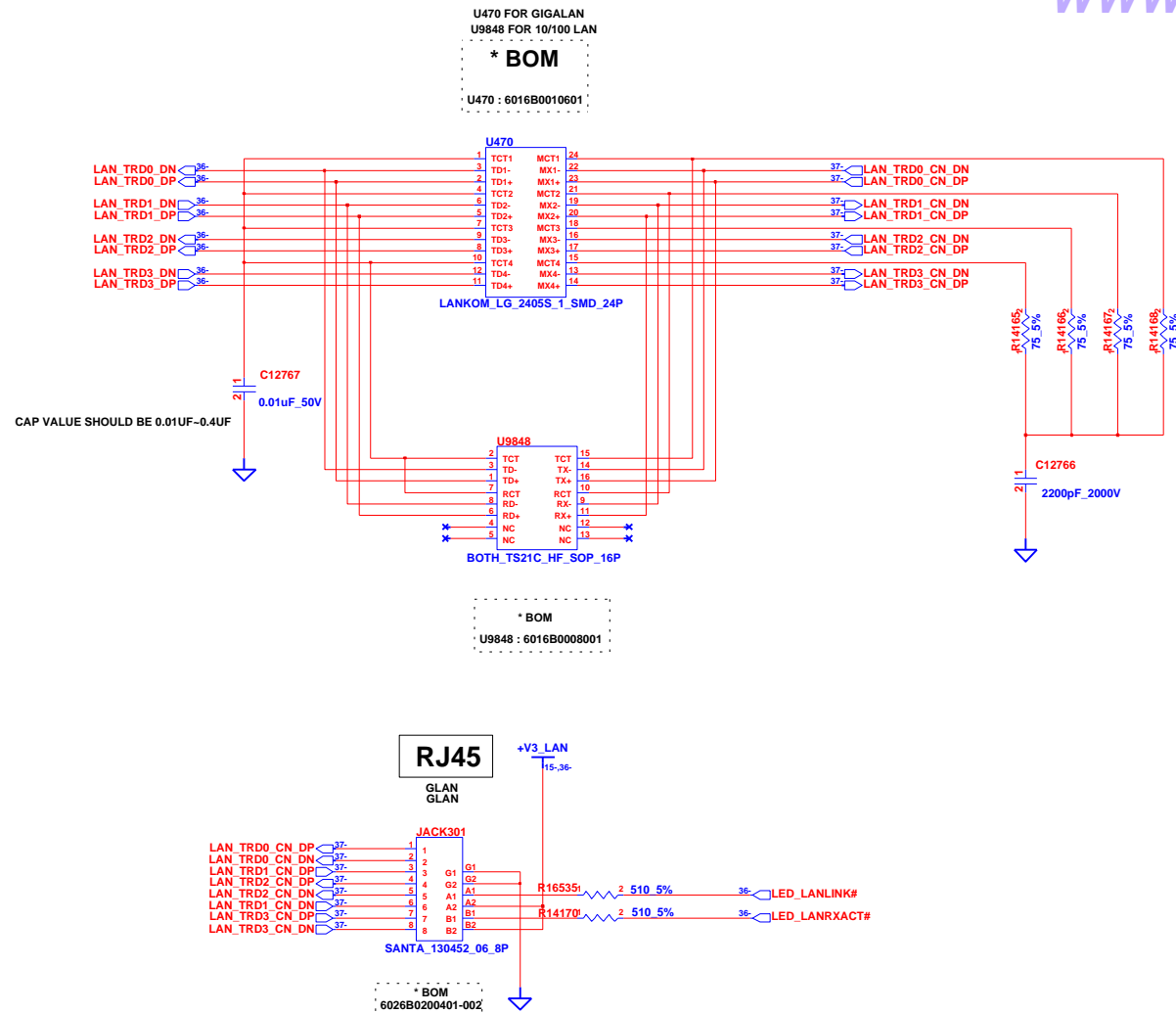
USB3.0_PORT



INVENTEC			
TITLE: <i>Surge 15.6 Brazos</i>			
SATA HDD & SATA DVD			
USB B CONN & PBN CONN			
SIZE: A3	CODE: CS	DOC NUMBER: 1310A24127-0-MTR	REV: B

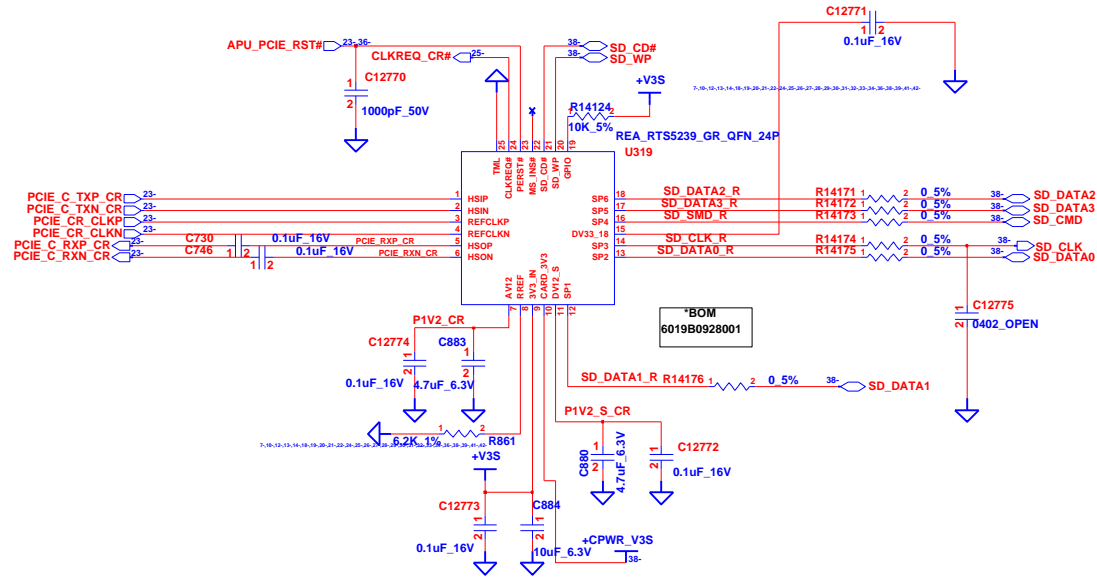
CHANGE by: *Chang, Irene* 6-Apr-2011

SHEET 35 OF 45

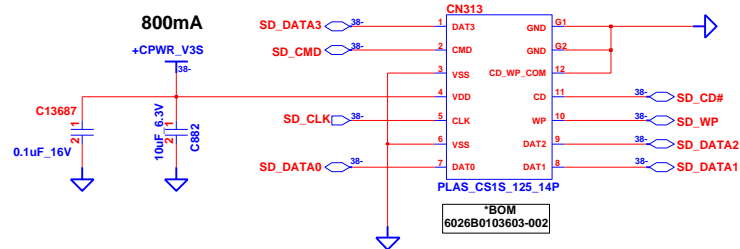


LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

INVENTEC			
TITLE Sarah 15.6 Brazos RTL8168EH			
SIZE A3	CODE CS	DOC. NUMBER 1310A24127-0-MTR	REV B
CHANGE by Chang, Irene		3-Oct-2011	
SHEET 37		OF 45	



Card Reader CONN



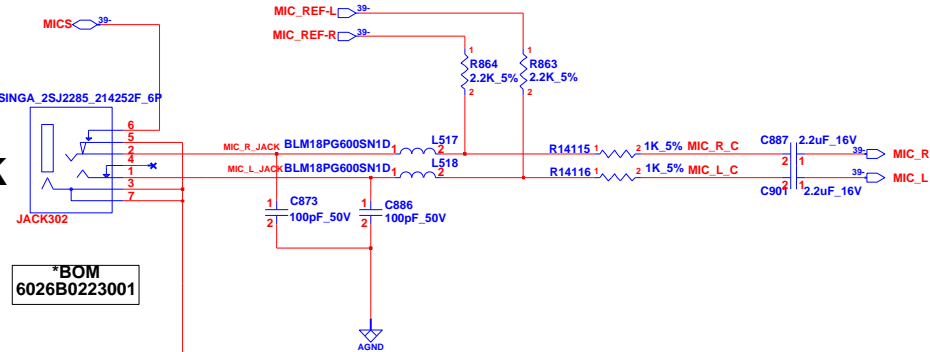
INVENTEC

TITLE			
Sarah 15.6 Brazos LAN & RJ45 CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B
SHEET		38	OF 45

CHANGE by Chang, Irene 7-Aug-2010

MIC JACK

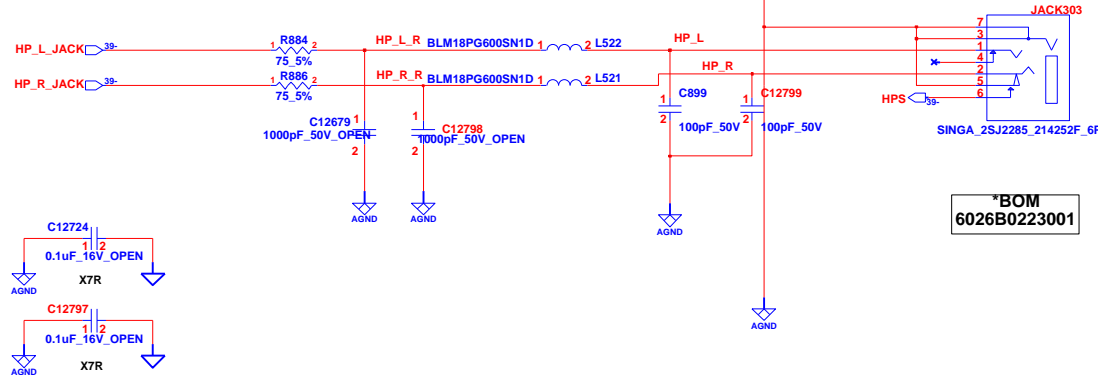
Normal OPEN



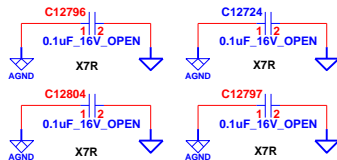
*BOM
6026B0223001

HP JACK

Normal OPEN



*BOM
6026B0223001



INVENTEC

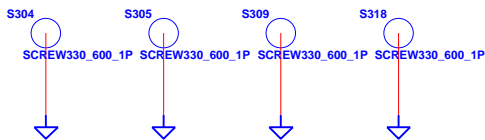
TITLE
Sarah 15.6 Brazos
AUDIO JACK

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B

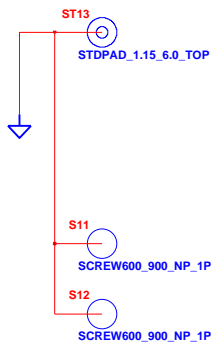
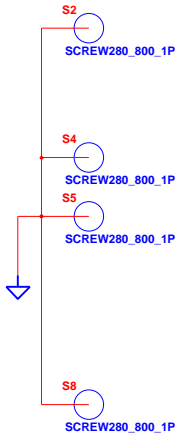
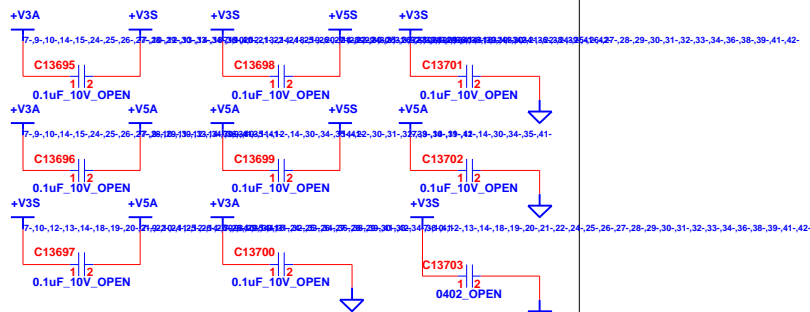
CHANGE by Chang, Irene 7-Aug-2010

SHEET 40 OF 45

For APU



For EMI CAP



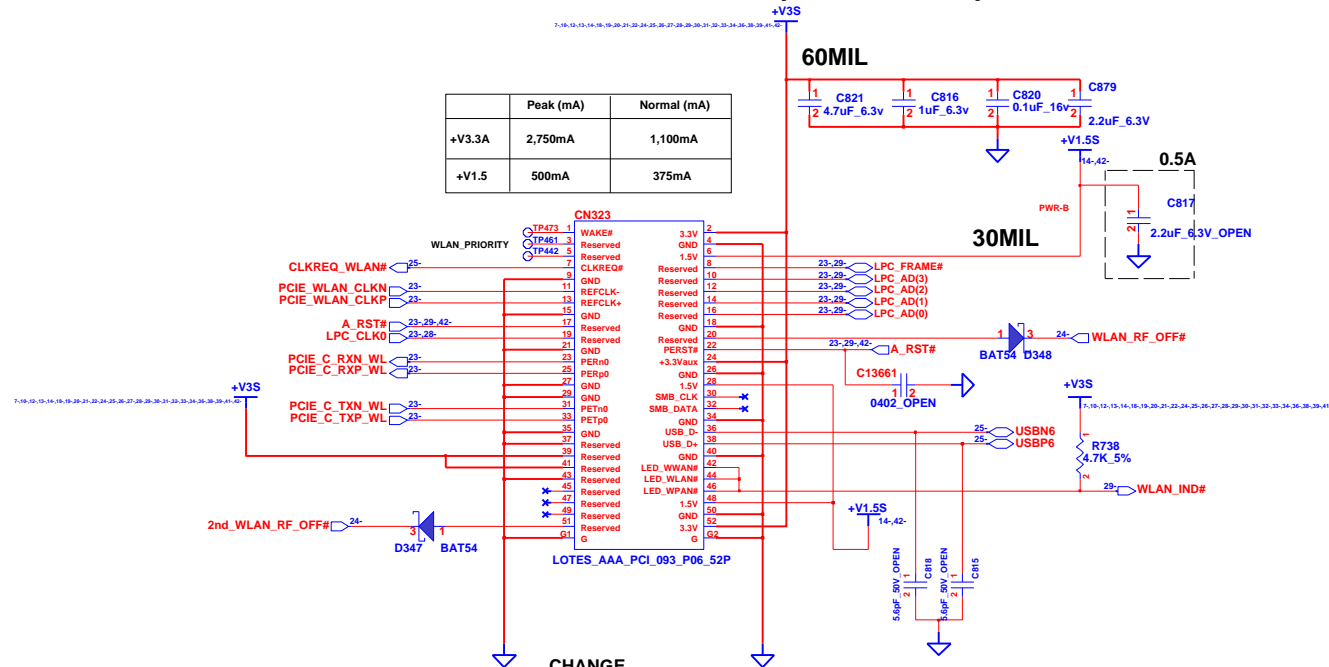
INVENTEC

TITLE Sarah 15.6 Brazos

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B
SHEET		41	OF 45

CHANGE by Chang, Irene 12-Mar-2011

WLAN CONN (MINICARD)



CHANGE

*BOM
CN323 : 6026B0184301

	FCH
WLAN_RF_OFF#	GPIO178
2nd_WLAN_RF_OFF#	GPIO180

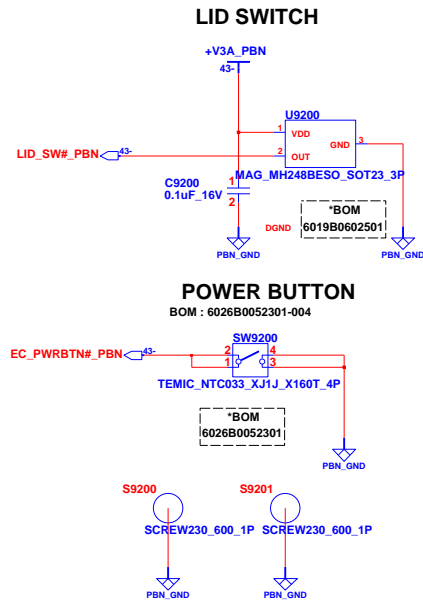
6026B0221502 SI BUILD

INVENTEC

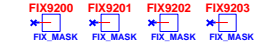
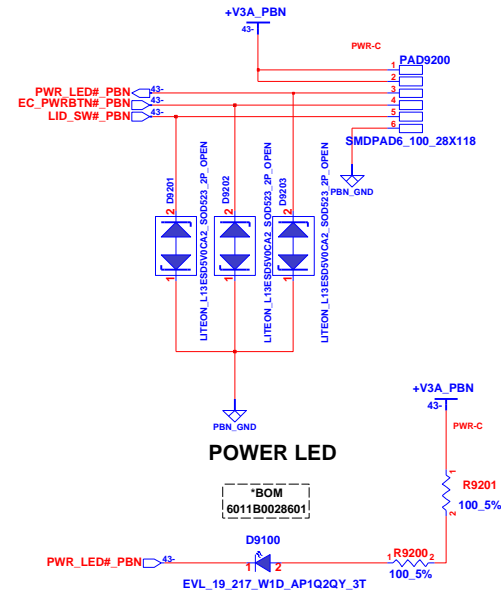
TITLE			
Sarah 15.6 Brazos			
SCREW			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B
SHEET		42	OF 45

CHANGE by *Chang, Irene* 1-Dec-2010

Power Button Board

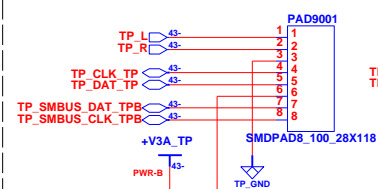


PBN Cable CN on PBN

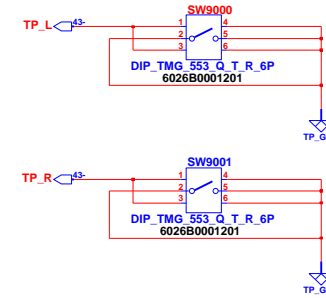
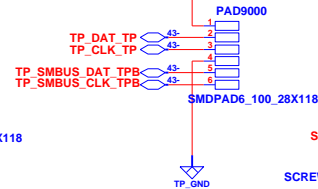


Pick-Button BOARD

TO T/P MODULE



TO MB



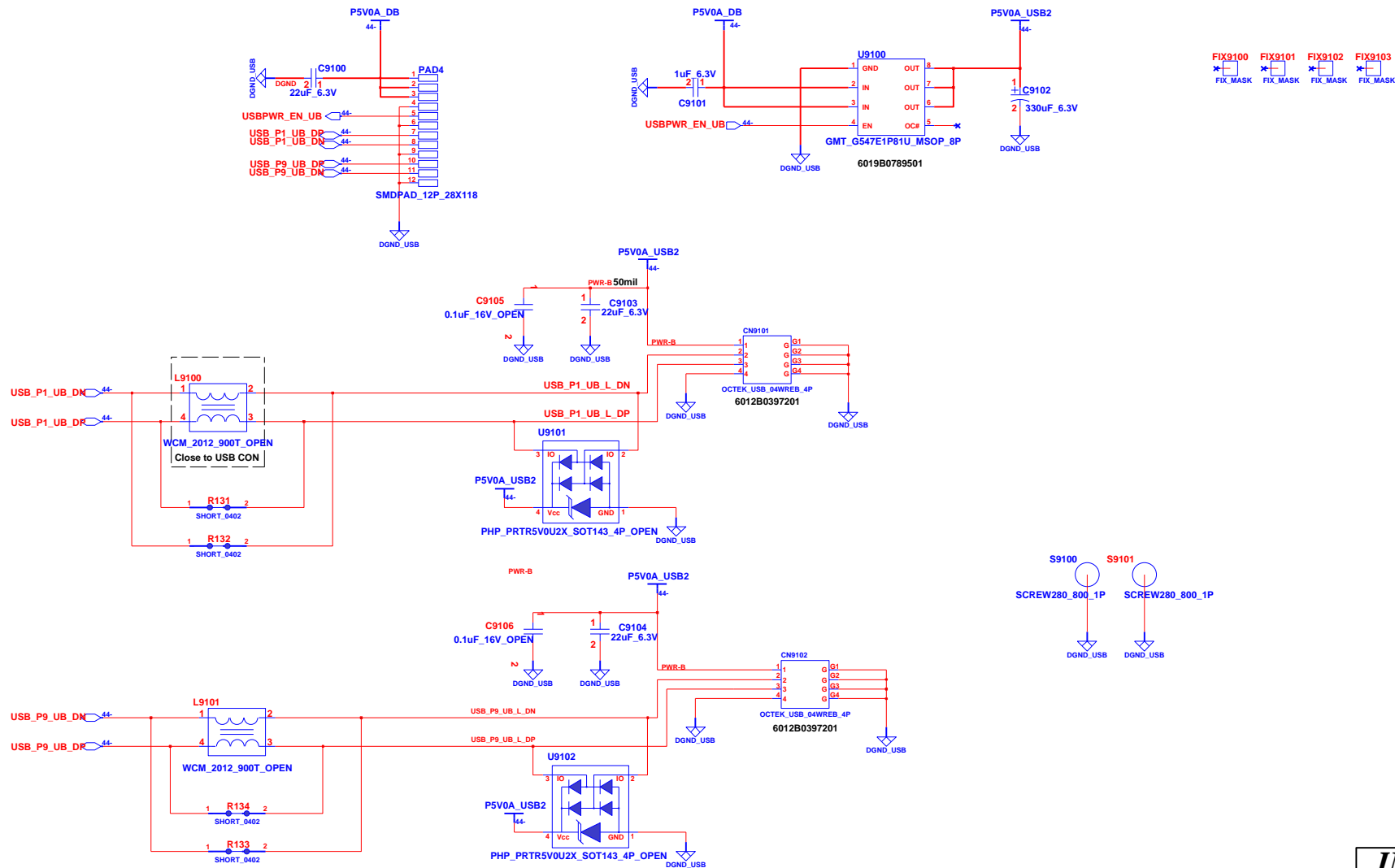
INVENTEC

TITLE			
Sarah 15.6 Brazos			
WLAN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A24127-0-MTR	B
SHEET		43	OF 45

CHANGE by Chang, Irene 23-Sep-2011

USB BOARD

WWW.AliSaler.Com

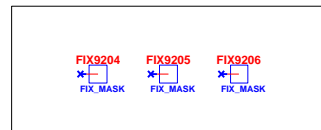
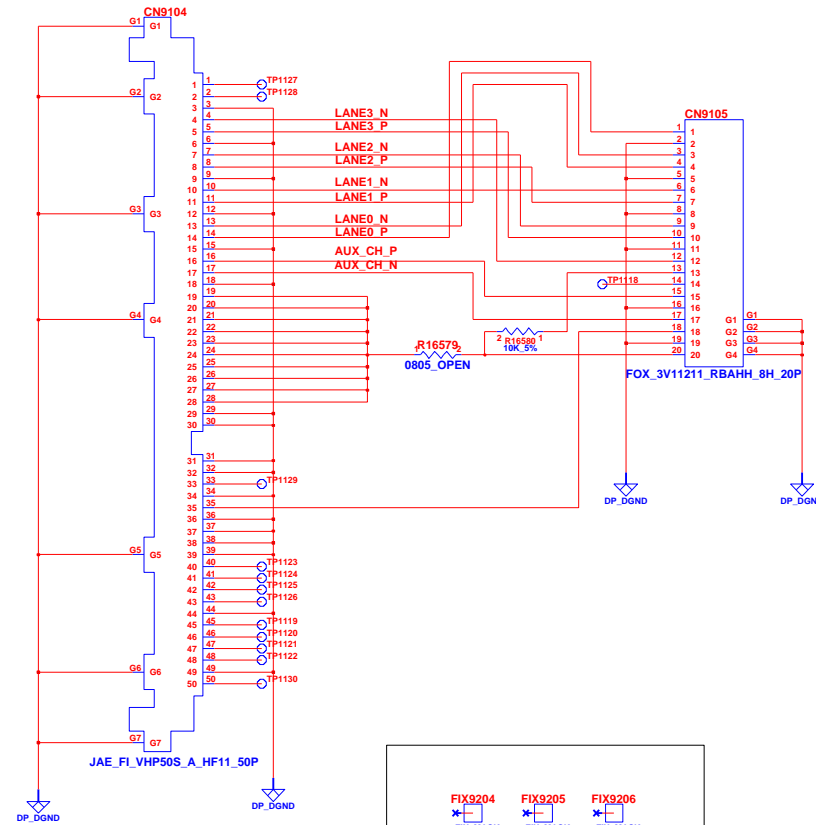


FIX9100
FIX9101
FIX9102
FIX9103

S9100
SCREW280_800_1P
S9101
SCREW280_800_1P

INVENTEC			
TITLE Sarah 15.6 Brazos STRAP			
SIZE A3	CODE CS	DOC. NUMBER 1310A24127-0-MTR	REV B
CHANGE by Chang, Irene		6-Apr-2011	
SHEET 44		OF 45	

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INVENTEC			
TITLE KF14BR-SCHE-DB-20110928-M3L			
SIZE A3	CODE CS	DOC. NUMBER	REV
SHEET 45		OF 45	

CHANGE by KF14BR 21-Oct-2011